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THE UNIVERSITY OF ALBERTA

TRANSISTORIZED OPERATIONAL AMPLIFIERS

by

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A THESIS

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ABSTRACT

This thesis report describes the design and construction of a transistorized operational amplifier which can be used either as a general purpose high performance amplifier or as a high speed analog computational device.

The design of the main amplifier is described showing the theoretical and practical considerations involved.

Subsequently a chopper stabilization channel is described which uses insulated gate field effect transistors as chopper and demodulator. The chopper channel shown was especially designed for this operational amplifier but it can easily be adapted for use with other amplifiers.

Lastly, a modification of the operational amplifier is described which uses either insulated gate or regular field effect transistors in the input stage. This greatly improves the holding mode operation if the amplifier is used as an integrator without chopper stabilization.

In the design of the entire amplifier, including the chopper stabilization channel, extensive use is made of feedforward principles. The use of these principles makes possible the attainment of very great bandwidth

together with reasonable power output to high frequencies while using readily available medium speed transistors.

ACKNOWLEDGEMENTS

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LIST OF SYMBOLS AND DEFINITIONS

s, - Laplace Transform Operator

$C(s)$, - Laplace Transform of Output Signal

$R(s)$, - Laplace Transform of Input Signal

$A(s)$, - Laplace Transform of Amplifier Gain or Transfer Function

ω_i, Ω_j, - Breakfrequencies or Pole and Zero Locations in Radians per Second in the s-Plane

f_k, - Break Frequencies or Corner Frequencies in Hz.

$A(j\omega)$, $A(\omega)$, - Fourier Transform of the Amplifier Transfer Function

$\left[h_{pq}\right]$, - Matrix of Hybrid Transistor Parameters

$\left[g_{rs}\right]$, - Matrix of Device Conductance Parameters

β, - Transistor Current Gain or h_{fe}

I_c, - Transistor Quiescent Collector Current

Other symbols as defined in text.

STATEMENT OF THE PROBLEM

Modern analog computational methods often involve the use of fast repetitive operation coupled with digital switching and mode control. An example of such methods is the use of hybrid computing in which an analog and a digital computer are used together. This type of application of analog equipment dictates the use of amplifiers that are capable of operating accurately at high frequencies.

The following specifications were therefore set for the amplifier described in this thesis report:

1. Plus or minus 10 Volt output capability at a 30 mAmp maximum load current.
2. The open loop unity gain frequency to be 100 MHz.
3. The input impedance at low frequencies to be 200 kOhms nominally.
4. The open loop D.C. gain to be a nominal 20,000 Volts per Volt.
5. Maximum output power to be available to frequencies as high as 1 MHz.
6. The entire high frequency roll-off slope not to exceed plus or minus 20 dB per decade asymptotically.
7. The amplifier to have a differential input for the purpose of applying chopper stabilization.

8. The input stage to be flexible enough so that either field effect or insulated field effect transistors instead of planar transistors may be used in the input stage.

For the chopper stabilization channel that is to be used with this amplifier the following specifications were set:

1. The available output voltage to be 0.2 Volts into a 200 kOhm load.
2. The D.C. open loop gain to be 1,000 minimum for a 200 kOhm load impedance.
3. The input impedance at D.C. to be 150 kOhms nominally.
4. The temperature characteristics of the entire stabilized operational amplifier to be 1 micro-Volt per degree Centigrade or better over an ambient temperature range of 20 degrees to 70 degrees Centigrade if referred to the input or summing junction.

The theory and methods of design and construction of such an amplifier will be discussed in the remainder of this report.

INTRODUCTION

Operational amplifiers which exhibit unity gain frequencies of 100 MHz can be constructed using conventional design methods. However, to carry out such a design compromises may have to be made which could limit the suitability of the amplifier for its intended purpose. The nature of the limitations and problems will here be discussed.

To arrive at a design with a unity gain frequency of 100 MHz it is necessary that the frequency response of each amplifier stage be controlled from D.C. to frequencies in excess of 100 MHz. This necessitates the use, in each stage, of transistors with unity beta frequencies greater than 100 MHz and with small values of collector to base capacity. The overall frequency response of such an amplifier may then be adjusted by control of the responses of the individual stages.

There are three normally used approaches to compensation:

1. All but one of the amplifier stages are arranged to have their corner frequencies as high as possible. The one excepted stage is then designed to have a dominant pole at a frequency which is low enough that all other amplifier

corner frequencies occur beyond the unity gain frequency of the amplifier.

2. Each amplifier stage is designed to have a frequency response with one or more poles and zeros in its roll-off characteristics. The responses of the various stages are staggered to produce a composite response with asymptotic slopes no greater than 40 dB per decade but which crosses the 0 dB gain axis at 20 dB per decade. To accomplish this one or more lead networks are used.
3. Each amplifier stage but one is designed to have a pole, a zero, and a pole, in that order to increasing frequencies in its response curve. One stage is designed to have only a pole in its transfer function. In this way all but one of the stages will have a zero slope section, a 20 dB per decade slope section, a zero slope section, and a 20 dB per decade slope section in its transfer function. The last 20 dB per decade slope section for each stage can be made to occur outside the unity gain frequency of the amplifier, and the first sloping sections can be staggered in such a way that the composite slope

inside the passband to the unity gain frequency is never greater than 20 dB per decade.

Korn and Korn(1) show that these methods of operational amplifier design, with possible variations, are practical for amplifiers with unity gain frequencies of 10 MHz or lower. Various attempts were made to use methods of this general type in the design of an amplifier with a unity gain frequency of 100 MHz, but during the progress of the work, several disadvantages to these methods became evident. These may be summarized as follows:

1. Special high frequency transistors are required for all stages.
2. Relatively small collector load resistors and high collector currents are necessary. This requires the use of transistors with considerable voltage and power ratings.
3. To satisfy conveniently the condition of zero D.C. output voltage for zero D.C. input voltage both npn and pnp transistors are useful. Transistors with the above specifications are presently not readily available in both pnp and npn configurations.
4. The use of high frequency transistors in the input stage does not lead to a design that is

desirable from the standpoint of noise.

5. It is difficult to avoid roll-off slope sections of 40 dB per decade as required per specifications.
6. The frequency shaping networks in the amplifier prevent the circuit from delivering full output power at the higher frequencies below the unity gain frequency of the amplifier.

The problems described here can be alleviated, at least in part, by a design technique which uses feedforward principles. This method is treated in detail by authors such as Deering(2), Koerner(3), Polonikov(4), Whitman(5), and others.

Essentially this method consists in feeding a portion of the frequency spectrum inside the passband of the amplifier (the high frequency portion) directly from the input to some of the later stages thus bypassing the initial stages. As a result, only the final stages need to be capable of handling the higher frequencies. The high frequency signals are therefore not deteriorated as much by saturation effects resulting from the roll-off networks.

Additional details of this method will be treated in a subsequent chapter.

CHAPTER ONE

FEEDFORWARD DESIGN THEORY

To make use of feedforward techniques in amplifier design, the system under consideration has to be divided into two sub-channels, a low frequency channel, and a wide-band channel. Consider, therefore, the following system (figure 1):

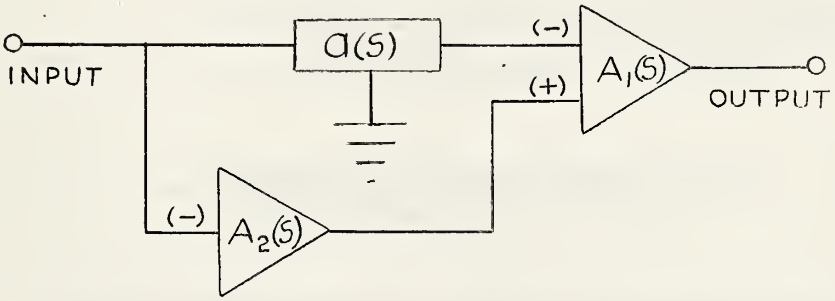

FIGURE 1. THE FEEDFORWARD SYSTEM

The overall transfer function for this system is:

$$\frac{C(s)}{R(s)} = A(s) = -A_1(s)\left[a(s) + A_2(s)\right] \tag{1.1}$$

Assume the following transfer functions for the blocks:

$$A_1(s) = A_1(o)\,\frac{\Omega_1\,\Omega_2}{(s+\Omega_1)(s+\Omega_2)} \tag{1.2}$$

$$A_2(s) = A_2(o)\,\frac{\omega_1 \cdots \omega_n}{(s+\omega_1)(s+\cdots)\cdots(s+\omega_n)} \tag{1.3}$$

where: $\Omega_1 < \Omega_2$

$$\omega_1 < \omega_2 < \cdots < \omega_n \tag{1.4}$$

and: $\Omega_1 > \omega_1$.

Then:

$$A(s) = A_1(o)\frac{\Omega_1\Omega_2 a(s)}{(s+\Omega_1)(s+\Omega_2)} + \frac{A_1(o)A_2(o)\Omega_1\Omega_2\omega_1 \cdots \omega_n}{(s+\Omega_1)(s+\Omega_2)(s+\omega_1)\cdots(s+\omega_n)}$$

$$= \frac{A_1(o)\Omega_1\Omega_2 a(s)(s+\omega_1)\cdots(s+\omega_n) + A_1(o)A_2(o)\Omega_1\Omega_2\omega_1\cdots\omega_n}{(s+\Omega_1)(s+\Omega_2)(s+\omega_1)\cdots(s+\omega_n)}$$

$$= \frac{\text{Constant} \times (n^{th}\text{order equation in } s)}{(s+\Omega_1)(s+\Omega_2)(s+\omega_1)\cdots(s+\omega_n)} \tag{1.5}$$

This transfer function offers the possibility of cancelling, by proper choice of breakfrequencies and gains, the effects of all but at least one of the poles of $A_2(s)$ and leaving the high frequency response determined purely by the poles of $A_1(s)$. This result is more clearly illustrated by the Bode plot of the system as in figure 2.

As a more detailed illustration consider the following case, using the system in figure 1 as an example:

Let the network represented by a(s) be such that in the frequency range of interest it can be assumed that:

$$a(s) \approx 1 \tag{1.6}$$

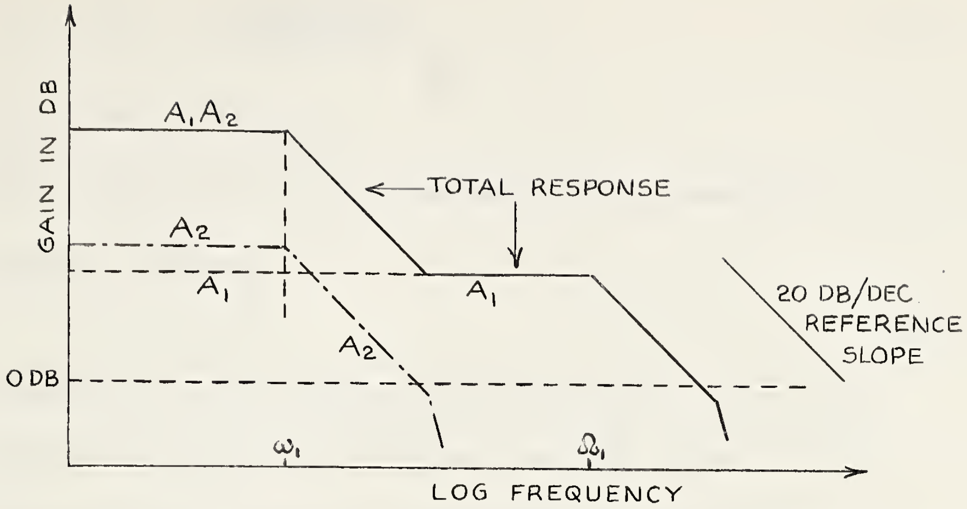

FIGURE 2. GENERAL FEEDFORWARD SYSTEM FREQUENCY RESPONSE

Suppose that the individual amplifiers with transfer functions $A_1(s)$ and $A_2(s)$ have their frequency responses rolled off by large capacitors in such a way that:

$$\begin{aligned} &\Omega_2 \gg \Omega_1 \\ &\omega_2 \text{ to } \omega_n \gg \omega_1 \end{aligned} \tag{1.7}$$

Then it can be assumed that:

$$A_1(s) = \frac{A_1(o)}{s+\Omega_1} = \frac{A_1}{s+\Omega_1} \tag{1.8}$$

$$A_2(s) = \frac{A_2\ (o)}{s+\omega_1} = \frac{A_2}{s+\omega_1} \tag{1.9}$$

where: $\omega_1 < \Omega_1$ (1.10)

Then, using formula 1.1:

$$\begin{aligned} -A(s) &= A_1(s)\left[a(s)+A_2(s)\right] \\ &= \frac{A_1}{s+\Omega_1}\left[1+\frac{A_2}{s+\omega_1}\right] = \frac{A_1(s+\omega_1+A_2)}{(s+\Omega_1)(s+\omega_1)} \end{aligned} \tag{1.11}$$

or: $$-A(s) = \frac{A_1(s+\omega_b)}{(s+\Omega_1)(s+\omega_1)} \qquad (1.11)$$

where: $\omega_b = \omega_1 + A_2$

This means that if ω_b is selected to lie between Ω_1 and ω_1 such that:

$$\omega_1 < \omega_b < \Omega_1 \qquad (1.12)$$

then the resulting system response will be of the form shown in figure 3. A frequency response curve of this nature is well suited to computational operational amplifiers.

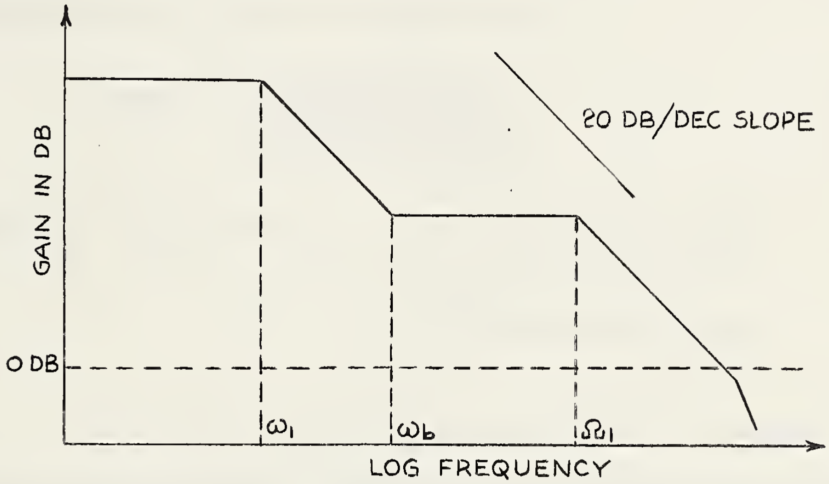

FIGURE 3. FEEDFORWARD AMPLIFIER RESPONSE

More generally, block a(s) is usually a simple RC high pass filter with transfer function:

$$a(s) = \frac{s}{s+\omega_a} \qquad (1.13)$$

If, as before, it is assumed that:

$$A_1(s) = \frac{A_1}{s+\Omega_1} \tag{1.8}$$

$$A_2(s) = \frac{A_2}{s+\omega_1} \tag{1.9}$$

and: $\omega_1 < \Omega_1$ (1.10)

then, substitution into formula 1.1 gives:

$$-A(s) = A_1(s)\left[a(s)+A_2(s)\right]$$

$$= \frac{A_1(s^2+\omega_1 s + A_2 s + A_2\omega_a)}{(s+\omega_1)(s+\Omega_1)(s+\omega_a)} \tag{1.14}$$

Expression 1.14 can be replaced by:

$$-A(s) = \frac{A_1(s+\Omega_3)(s+\Omega_4)}{(s+\Omega_1)(s+\omega_1)(s+\omega_a)} \tag{1.15}$$

where: $(s+\Omega_3)(s+\Omega_4) = (s^2+\omega_1 s+A_2 s+A_2\omega_a)$

$$= s^2+(\omega_1+A_2)s+A_2\omega_a \tag{1.16}$$

The pair of roots Ω_3, Ω_4 can be real or complex. To maintain roll-off slopes of plus or minus 20 dB per decade or less at all frequencies below the unity gain frequency the possibility of complex zeros must be excluded. Proper selection of ω_1, ω_a, and A_2 will accomplish this since:

$$\Omega_{3,4} = \frac{-(\omega_1+A_2)\pm\sqrt{(\omega_1+A_2)^2-4\,A_2\omega_a}}{2} \tag{1.17}$$

merely requires that:

$$(\omega_1 + A_2)^2 - 4\ A_2\omega_a > 0$$

or:

$$\omega_a < \frac{(\omega_1 + A_2)^2}{4\ A_2} \qquad (1.18)$$

Under condition 1.18 the Bode plot of the entire amplifier will be shown as in figure 4. It is desirable to eliminate the rising response between Ω_3 and ω_a in figure 4. This can be achieved as follows:

The system transfer function is expressed in formulae 1.14 and 1.15. A pole and a zero may be cancelled from this transfer function by setting:

$$(s+\Omega_3) = (s+\omega_a) \qquad (1.19)$$

Select Ω_3 as the zero closest to the origin. Then:

$$\Omega_3 = \frac{-(\omega_1 + A_2) + \sqrt{(\omega_1 + A_2)^2 - 4\ A_2\omega_a}}{2} \qquad (1.20)$$

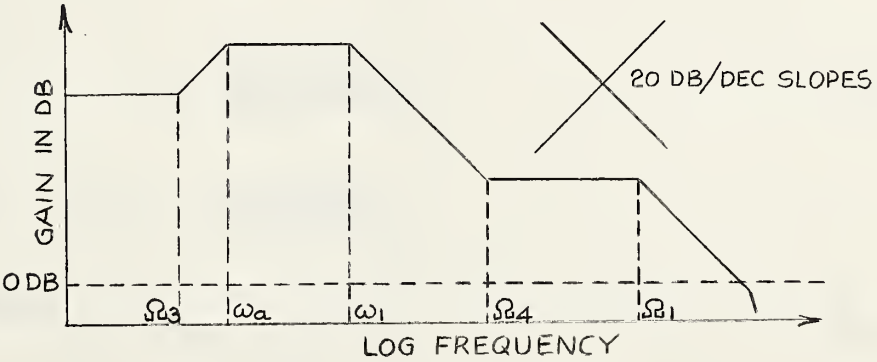

FIGURE 4. FEEDFORWARD AMPLIFIER RESPONSE WITH $a(s) \neq 1$

Equating:

$$-\omega_a = \frac{-(\omega_1 + A_2) + \sqrt{(\omega_1 + A_2)^2 - 4\,A_2\omega_a}}{2}$$

or: $$(\omega_1 - 2\omega_a + A_2)^2 = (\omega_1 + A_2)^2 - 4\,A_2\omega_a$$

Expanding and cancelling equal factors gives:

$$-4\omega_1\omega_a + 4\omega_a^2 = 0$$

And since $4\omega_a \neq 0$ it follows that:

$$\omega_a = \omega_1 \qquad (1.21)$$

is the required condition for eliminating a pole and a zero and thus removing the rising portion in the frequency response. Under condition 1.21 the system transfer function becomes:

$$-A(s) = \frac{A_1\left\{s^2 + (\omega_1 + A_2)s + A_2\omega_a\right\}}{(s+\Omega_1)(s+\omega_1)(s+\omega_a)}$$

$$= \frac{A_1\left\{(s + A_2)(s+\omega_a)\right\}}{(s+\Omega_1)(s+\omega_a)(s+\omega_a)}$$

$$= \frac{A_1(s + A_2)}{(s+\Omega_1)(s+\omega_a)} \qquad (1.22)$$

or: $$-A(s) = \frac{A_1(s+\Omega_4)}{(s+\Omega_1)(s+\omega_1)}$$

where:

$$\Omega_4 = A_2; \quad \omega_a = \omega_1 \qquad (1.23)$$

Figure 5 now shows the final Bode plot of the system.

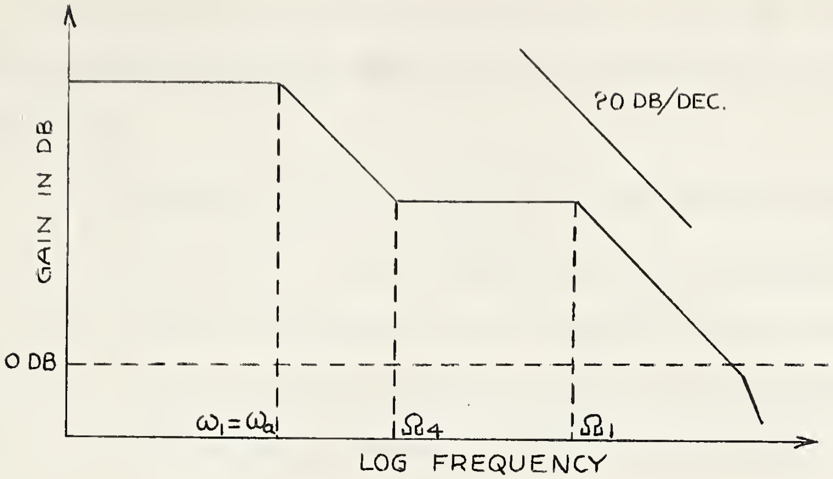

FIGURE 5. FINAL FEEDFORWARD SYSTEM RESPONSE

Since the amplifier to be designed along these lines is required to be suitable for use as a summer, integrator, or differentiator, the phase shift and gain roll-off should obey:

$$\begin{aligned}&|\text{Phase Shift}| \leqslant 90^\circ \\ &\text{Roll-off Slope} \leqslant 20 \text{ dB per decade}\end{aligned} \tag{1.24}$$

At the unity gain frequency Ω_4 of amplifier A_2 there may be a phase shift contribution of 90° from A_2. If, at this same frequency, there is also a considerable phase contribution from A_1, then the path $A_2 \rightarrow A_1$ may become unstable, or, at least, cancellation of the feedforward signals may occur. For this reason Ω_1 and Ω_4 may not be made to coincide.

In view of the above considerations, Korn and Korn$^{(1)}$ give the following design criteria for a feedforward system (figure 1):

1. The phase shift arg $A_2(j\omega)$ should be kept below 90° to 150° at all frequencies where $A_2(j\omega) \gg 1$. Therefore the Bode plot of $|A_2(j\omega)|$ should cross 0 dB at 20 dB per decade and any slopes greater than 40 dB per decade should be avoided above 9 dB.
2. Gain $|A_2(j\omega)|$ should drop to unity before phase shift due to $A_1(j\omega)$ becomes appreciable, say below one-fifth of the first breakfrequency of $A_1(j\omega)$.

Experimentation has shown that $|A_2(j\omega)|$ can be allowed to drop to unity at one-half of the first breakfrequency of $A_1(j\omega)$.without signs of instability provided $|A_2(j\omega)|$ rolls off to its unity gain frequency at a slope no greater than 20 dB per decade (see equation 1.24). The latter is the condition adhered to in the design of the amplifier in this report.

Feedforward amplifiers need not be limited to one feedforward loop. In figure 1. amplifier A_2 may, itself, consist of a complete feedforward system. A higher frequency amplifier A_1 may be added using the same design

principles for blocks A_2 and A_1 as outlined in this chapter for the case of A_2 not being a feedforward system.

It is to be noted that chopper stabilization of an operational amplifier that has a differential input is merely a special case of feedforward use. The main operational amplifier corresponds to block A_1 (figure 1) and the chopper channel corresponds to A_2. The design principles of this chapter, once again, apply. However, for reasons presented in a later chapter, the chopper channel frequency response cannot be allowed to roll off at 20 dB per decade. A 40 dB per decade slope section has to be tolerated. The chopper channel frequency response will therefore be arranged in accordance with the requirements set forth by Korn and Korn(1). The chopper amplifier frequency response will be arranged to drop to unity at one-fifth of the first break-frequency of the main amplifier.

CHAPTER TWO

THE OPERATIONAL AMPLIFIER

The previously set specifications for the amplifier in this project require that:

1. The input stage be differential with an input impedance at low frequencies of 200 kOhms.
2. The D.C. open loop gain be at least 20,000.
3. The amplifier be capable of producing plus or minus 10 Volts across a 330 Ohm load resistor.
3. Feedforward be used.

These objectives are met by using three stages of amplification and a complementary emitter follower output stage as depicted in figure 6. The output stage consists of a complementary emitter follower driven by a common collector stage.

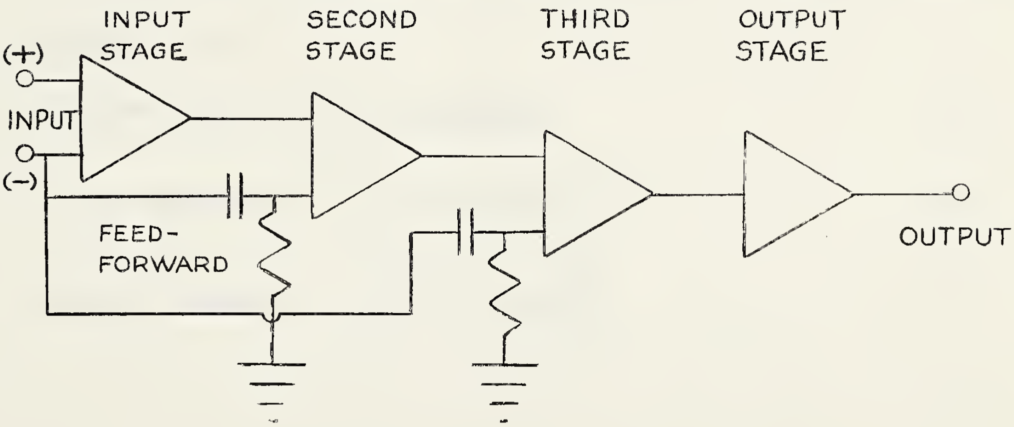

FIGURE 6. OPERATIONAL AMPLIFIER BLOCK DIAGRAM

The second and third stages are complementary differential stages of which the negative inputs are used as feedforward inputs. Complementary differential stages require no emitter current sources and the circuit is thus simplified. The input stage is differential and uses compound transistors to increase the gain and the input impedance.

Before gain and performance calculations can be carried out certain equations have to be presented. In most cases approximate gain and input impedance formulae are adequate (6) (7).

For all stages, the parameter h_{ib} can be found from:

$$h_{ib} \approx \left(\frac{26 \text{ mV}}{I_c \text{ (in mA)}} + 1.5 \right) \text{ Ohms} \qquad (2.1)$$

where I_c is the collector current.

For an emitter follower as shown in figure 7 the performance formulae are:

Voltage Gain: $$\text{V.G.} \approx \frac{1}{1 + h_{ib}/R_L} \qquad (2.2)$$

Input Impedance: $$R_{in} \approx \beta h_{ib} + \beta R_L \qquad (2.3)$$

Output Impedance: $$R_{out} \approx h_{ib} + \frac{R_s}{\beta} \qquad (2.4)$$

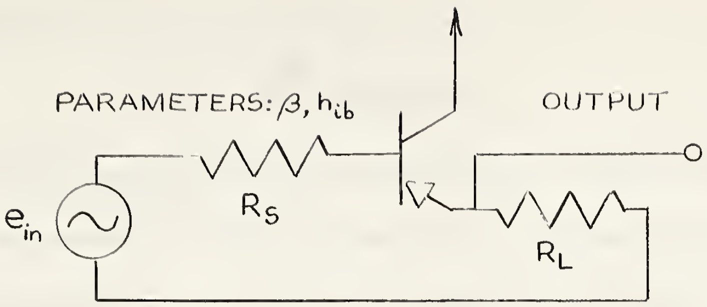

FIGURE 7. THE EMITTER FOLLOWER

For a differential stage, either regular or complementary as shown in figure 8:

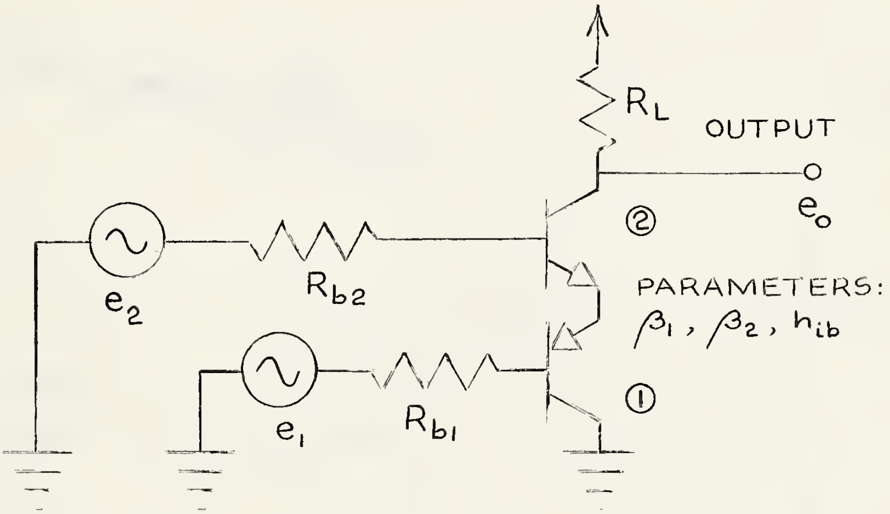

FIGURE 8. THE DIFFERENTIAL STAGE

Voltage Gain:

$$V.G.(1) = \frac{e_o}{e_1} \approx \frac{R_L}{2h_{ib} + \frac{R_{b2}}{\beta_2}}$$

$$V.G.(2) = \frac{e_o}{e_2} \approx \frac{R_L}{2h_{ib} + \frac{R_{b1}}{\beta_1}} \qquad (2.5)$$

Input Impedance: $R_{in}(1) \approx 2\beta_1 h_{ib} + R_{b2}$

$$R_{in}(2) \approx 2\beta_2 h_{ib} + R_{b1} \qquad (2.6)$$

In the input differential stage use is made of a compound transistor. The configuration is shown in figure 9. Its approximate equivalent h-parameters in terms of the parameters of the individual transistors are given by:

$$h_{fe} = \beta \approx h_{fe}^{(1)}\ h_{fe}^{(2)*} \qquad (2.7)$$

$$h_{ib} \approx \frac{h_{ib}^{(1)}}{h_{fe}^{(2)*}} \qquad (2.8)$$

where: $$h_{fe}^{(2)*} \approx \frac{R_A\ h_{fe}^{(2)}}{h_{ib}^{(2)} h_{fe}^{(2)} + R_A} \qquad (2.9)$$

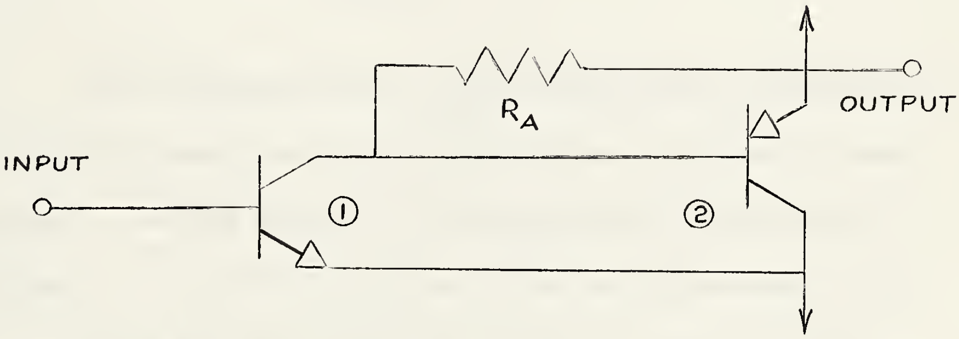

FIGURE 9. THE COMPOUND TRANSISTOR

The exact equivalent h-parameter formulae, where the common collector parameters for the second transistor include the effects of resistor R_A, are:

$$h_{ie} = \frac{h_{ie}^{(1)}(1+h_{ic}^{(2)}h_{oe}^{(1)}) - h_{fe}^{(1)}h_{ic}^{(2)}h_{re}^{(1)}}{1+h_{ic}^{(2)}h_{oe}^{(1)}} \qquad (2.10)$$

$$h_{fe} = \frac{-h_{fe}^{(1)}h_{fc}^{(2)}}{1+h_{ic}^{(2)}h_{oe}^{(1)}} \qquad (2.11)$$

$$h_{re} = \frac{h_{re}^{(1)}h_{rc}^{(2)}}{1+h_{ic}^{(2)}h_{oe}^{(1)}} \qquad (2.12)$$

$$h_{oe} = h_{oc}^{(2)} - \frac{h_{rc}^{(2)}h_{oe}^{(1)}h_{fc}^{(2)}}{1+h_{ic}^{(2)}h_{oe}^{(1)}} \qquad (2.13)$$

The output impedance of a common emitter stage is:

$$R_o = \frac{1}{h_{oe} - \frac{h_{re}h_{fe}}{h_{ie}+R_s}} \qquad (2.14)$$

The characteristics of the complementary differential stage with feedforward input need to be considered in more detail. Let the simplified configuration be that shown in figure 10. In this figure the following definitions hold:

R_L is the effective load resistor composed of the parallel combination of the collector load resistor and the input resistance of the next stage.

R_b is the parallel combination of the bias resistors.

R_c is the collector load resistor of the previous stage.

C_b is the roll-off capacitor of this stage.

C_f is the feedforward capacitor.

C_a is the roll-off capacitor of the previous stage.

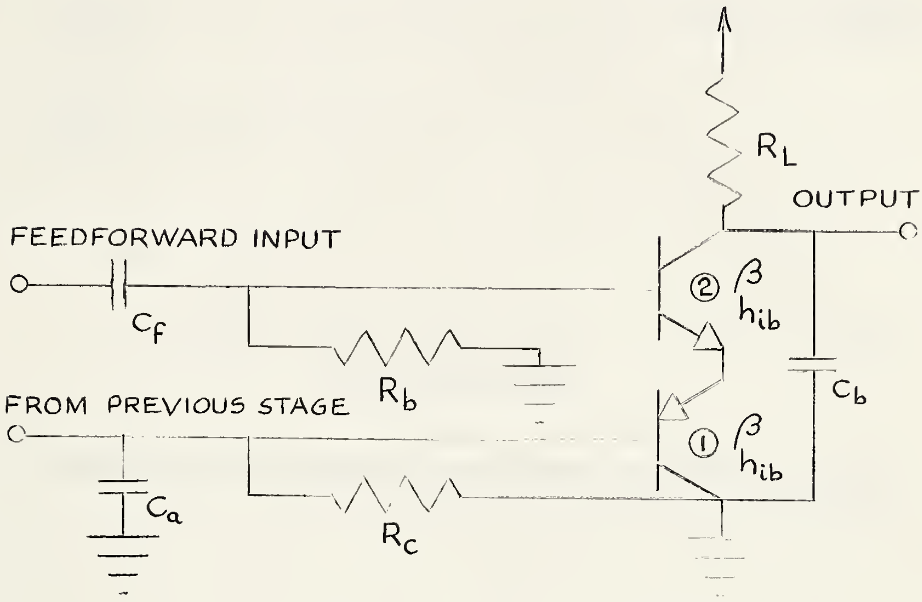

FIGURE 10. THE DIFFERENTIAL STAGE WITH FEEDFORWARD

The frequency response of the feedforward input of the complementary differential stage is shown in figure 11. and the response of the regular input connected directly to the previous stage is shown in figure 12. The feedforward input frequency response will comply with the requirements set out in chapter one if the corner frequency of the feedforward network is chosen to occur at a frequency that coincides with or is slightly smaller than the frequency of the zero in the feedforward response.

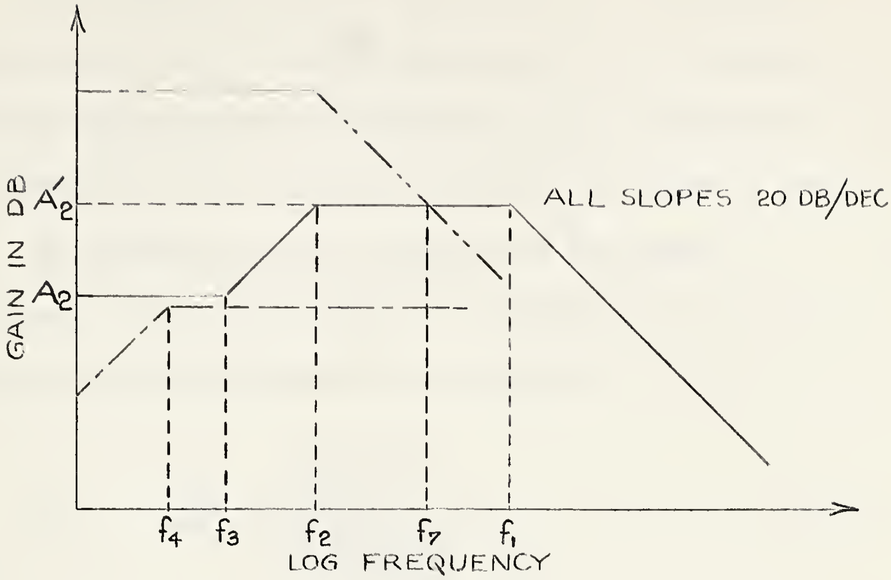

FIGURE 11. THE FEEDFORWARD INPUT FREQUENCY RESPONSE

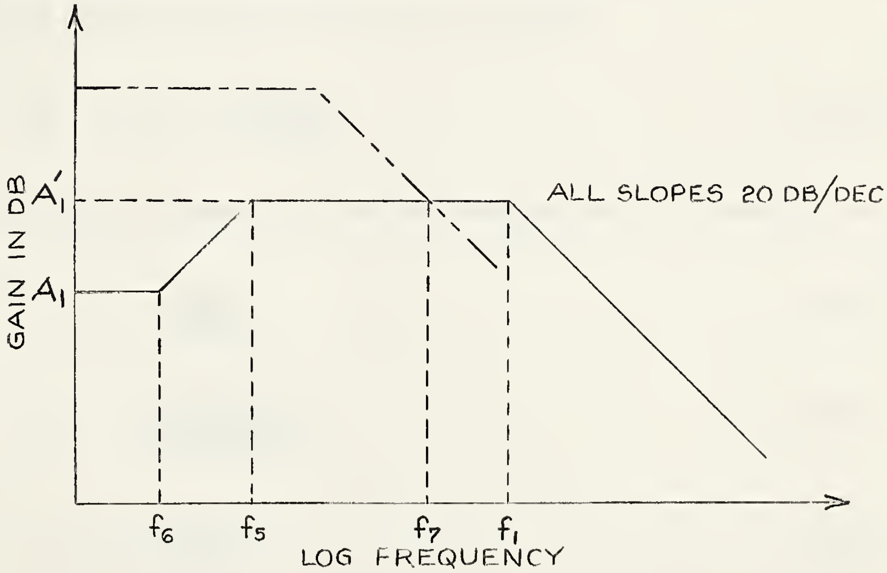

FIGURE 12. THE REGULAR INPUT FREQUENCY RESPONSE

The change in low frequency gain of the regular input from A_1 to A_1' is undesirable but is partly compensated for by an equivalent increase in input impedance which results in an increase in gain of the previous stage.

By substituting into formula 2.5 the actual impedances of the base networks consisting of C_a, R_c, C_f, and C_b the following formula is obtained:

$$\text{V.G.} = \frac{R_L}{2h_{ib}} \times \frac{\left(\frac{1}{R_b C_f} + s\right)}{\left(\frac{2\beta h_{ib} + R_b}{2\beta h_{ib} R_b C_f} + s\right)} \tag{2.15}$$

This is the expression for the regular input. The gain expression for the feedforward input is similar with R_b and C_f replaced by R_c and C_a. On the basis of equation 2.15, the following results can be derived:

$$A_1' = A_2' = \frac{R_L}{2h_{ib}} \tag{2.16}$$

Gains A_1 and A_2 can still be obtained by use of formula 2.5.

Also:

$$f_1 = \frac{1}{2\pi C_b R_L} \tag{2.17}$$

$$f_2 = \frac{2\beta h_{ib} + R_c}{4\pi\beta h_{ib} R_c C_a} \tag{2.18}$$

$$f_3 = \frac{1}{2\pi R_c C_a} \tag{2.19}$$

$$f_5 = \frac{2\beta h_{ib} + R_b}{4\pi\beta h_{ib} R_b C_f} \qquad (2.20)$$

$$f_6 = \frac{1}{2\pi R_b C_f} \qquad (2.21)$$

Frequency f_7 (figures 11 and 12) is the required unity gain frequency of the previous stage and is related to the others by the requirement based on feedforward theory:

$$f_7 \ll \tfrac{1}{2} f_1 \qquad (2.22)$$

The input impedance to either input is still given by equations 2.6 but the effective value of R_b is either R_b or zero depending on whether frequencies above or below the corner frequency of the respective RC network are being considered.

The design of the amplifier can now be carried out. The complete amplifier circuit diagram is shown in figure 13. and will be referred to regularly in the next sections.

THE OUTPUT STAGE

A complementary emitter follower output stage was chosen to minimize the quiescent power supply current and power dissipation in the output transistors. The emitter followers also provide a relatively low open loop output impedance.

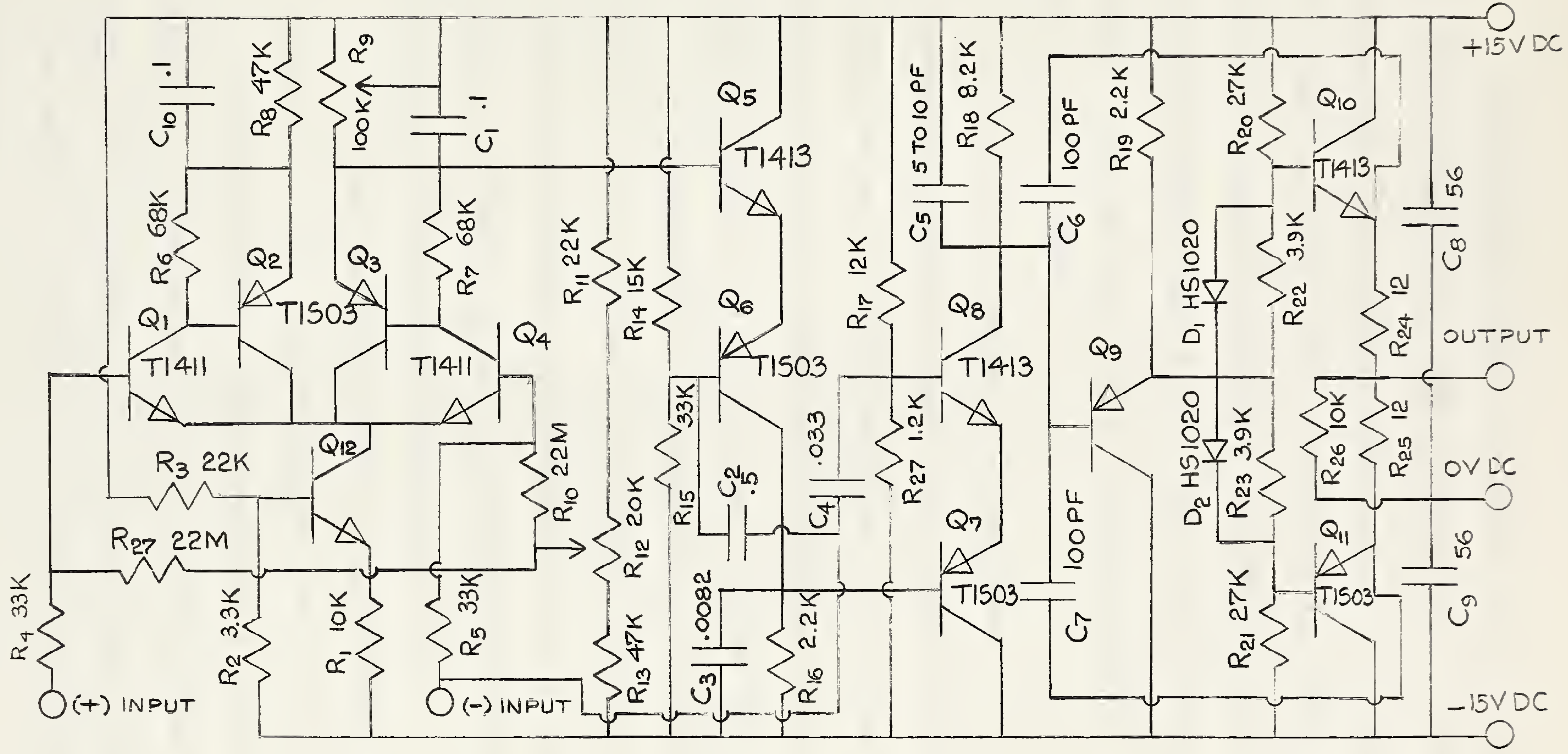

FIGURE 13. THE COMPLETE OPERATIONAL AMPLIFIER CIRCUIT

Resistor R_{26} (figure 13) makes the stage operate properly in the absence of an external load. Diodes D_1 and D_2 reduce the crossover distortion. The current in the diodes is set by means of resistors R_{20} and R_{21}. The diode current is adjusted to 0.5 mAmps which is larger than the maximum signal base current of Q_{10} and Q_{11}. Resistors R_{24} and R_{25} set the quiescent current in Q_{10} and Q_{11} to 0.4 mAmps.

The input resistance and capacitance of the complementary emitter follower vary widely depending on load resistance and signal amplitude. To isolate the previous stages from these severe impedance variations a common collector stage Q_9 is used to drive Q_{10} and Q_{11}.

As a side effect, resistors R_{19}, R_{20}, and R_{21}, form two voltage dividers which together with the action of the diodes may reduce the maximum available output voltage. Resistors R_{22} and R_{23}, which reduce this effect, are active for large signal amplitudes only.

From the transistor data sheets, an average value of 70 is chosen for β. Then by repeated use of formulae 2.1, 2.2, and 2.3 the output stage gain is found to vary from 0.88 to 0.99 for no load and 470 Ohm external load conditions respectively. The equivalent input impedances to the stage are 135 kOhms and 125 kOhms for the same load conditions.

The emitter followers used in the output stage tend to contribute a considerable amount of phase shift at frequencies beyond 30 MHz. Such phase shifts can make the amplifier unstable. To reduce these phase shifts, feed-forward is applied via capacitors C_6 and C_7 from the stage input directly to the output. Since C_6 and C_7 are effectively bootstrapped, they contribute at the most, 10 pf to the input capacity of the output stage at frequencies below 10 MHz. The output stage input capacity lies in the range of 15 pf to 25 pf.

THE THIRD STAGE

The third stage is a complementary differential amplifier consisting of Q_7 and Q_8 (figure 13). The regular input signal from the previous stage (direct coupled) is introduced at the base of Q_7; and the feed-forward signal is fed into the base of Q_8. The base of Q_8 is biased to about minus 12.5 Volts to allow maximum output voltage swing.

The collector current in this stage is 1.9 mAmps which, by formula 2.1, predicts a value of 15.1 Ohms for h_{ib}. An average value of 70 was obtained from the data sheets for the current gain of the transistors used. Combining the collector resistor with the input impedance

of the output stage produces an effective load resistance for the third stage of 7.8 kOhms. The equivalent parallel resistance of the bias network of Q_8 is 1.09 kOhms. Further calculations of stage performance may now be carried out.

Formula 2.16 yields the high frequency gain of either input (R_b equals 0 Ohms) as 258 (A_1' or A_2' in figures 11 or 12). The major corner frequency of the stage was, therefore, set to 500 KHz by means of the parallel combination of C_5 and the input capacity of the output stage.

The unity gain frequency of the second stage should be one-half of the major corner frequency of the third stage or 250 KHz. Since the feedforward gain of the second stage, as calculated in the next section, is 13,the major corner frequency of the second stage should be 19.2 KHz.

By formula 2.6, the high frequency input impedance (R_b equals 0 Ohms) to Q_7 in parallel with collector resistor R_{16} yields a collector impedance level of 1.08 kOhms. Capacitor C_3 is selected as 0.0082μf to produce an approximate roll-off corner frequency of 19 KHz for the second stage.

Once the value of capacitor C_3 is known, corner frequency f_3 (figure 11) can be calculated from formula 2.19 and is 8.9 KHz. The low frequency input impedance calculated from equation 2.6 and combined with the biasing

network resistance yields an impedance level at the base of Q_8 of 870 Ohms. Therefore feedforward capacitor C_4 is chosen as 0.033μf to give a corner frequency slightly lower than 8.9 KHz as required.

The D.C. gain of the third stage, also given by formula 2.5, is 170.

THE SECOND STAGE

The configuration of the second stage is equal to that of the third stage. Its operation is therefore analogous. The base of Q_6 is the feedforward input and the base of Q_5 is the regular or low frequency input which is direct coupled to the previous stage. The base of Q_6 is biased to plus 5.90 Volts to allow the collector D.C. level of the input stage to lie halfway between its effective supply voltages.

The collector current of the second stage is 650 μAmps and the current gain value used is 70. By formula 2.1 the value of h_{ib} is thus 41.5 Ohms. Combining the collector load resistor with the input impedance of the third stage yields an effective high frequency load impedance of 1.08 kOhms and a low frequency load impedance of 1.30 kOhms. The effective biasing network resistance at the base of Q_6 is 10.3 kOhms.

From the data presented, the feedforward gain of the second stage is calculated to be 13 using equation 2.5 with R_b equal to zero.

The low and high frequency input impedances at the base of Q_5, obtained from equation 2.6, are 16.1 and 5.81 kOhms respectively. In the next section, the gain of the input stage, looking into a load of 5.81 kOhms is shown to be 40, while the first stage output impedance calculated there is 43.1 kOhms. The required breakfrequency of the first stage is found by dividing one-half of the major corner frequency of the second stage by the first stage gain. The resulting break frequency is 270 Hz. Roll-off capacitor C_1 was therefore chosen to be 0.1 μf on the basis of the high frequency impedance level at the collector.

The zero in the feedforward gain of the second stage occurs at about 35 Hz (from formula 2.19). The input impedance to Q_6, including the bias network, is 8.5 kOhms. Feedforward capacitor C_2 was therefore selected as 0.5 μf.

The D.C. gain of the second stage, as obtained from equation 2.6, is 5.7.

THE INPUT STAGE

The input stage is a differential configuration which uses two compound transistor blocks as amplifiers with a transistor current source in the emitters. The use of

compounds increases both the gain and the input impedance of the stage. Referring to figure 13, the base of Q_1 corresponds to the positive amplifier input while the base of Q_4 is the negative amplifier input. Resistors R_6 and R_7 set the collector current in the input transistors to about 10 μAmps. The total collector current per side is determined by the current source Q_{12} and is 165 μAmps. Adjustment in the relative sizes of R_6 and R_7 may be necessary to compensate for differences in V_{be} of the input transistors.

The approximate h-parameters for the transistors of the input stage measured and/or calculated at their respective operating points are:

Q_1 and Q_4:	Q_2 and Q_3:
$h_{fe} = 25$	$h_{fe} = 60$
$h_{ie} = \beta h_{ib} = 65$ kOhms	$h_{ie} = \beta h_{ib} = 8.4$ kOhms
$h_{re} = 5 \times 10^{-5}$	$h_{re} = 8 \times 10^{-5}$
$h_{oe} = 5 \times 10^{-7}$ mhos	$h_{oe} = 5 \times 10^{-6}$ mhos

By first correcting the h-parameters of Q_2 and Q_3 for the insertion of R_6 and R_7, the equivalent h-parameters for the compound may be calculated from formulae 2.10, 2.11, 2.12, and 2.13. These parameters become:

$h_{fe} = 1330$

$h_{re} = 5 \times 10^{-5}$

$h_{ie} = 144$ kOhms

$h_{oe} = 2.3 \times 10^{-6}$ mhos

With the aid of these parameters, the output impedance of the input stage may be calculated. Since the output impedance of transistors Q_1 and Q_2, considered as a common collector amplifier, appears as an equivalent emitter resistor for negative input transistors Q_3 and Q_4 a correction needs to be made. The common collector output impedance of Q_1 and Q_2 combined is calculated from equation 2.14 as 73 Ohms. An equivalent resistance $\beta \times 73$ Ohms is added to h_{ie} for the compound and the new parameter values are substituted into equation 2.14 once again. This yields the output impedance of the input stage as approximately 500 kOhms. Since the output impedance thus calculated is very much dependent upon h_{re} it was checked by measurement. The measured value of output impedance was 440 kOhms.

The gain and the input impedance of the input stage may be calculated using approximate formulae. Equations 2.1, 2.7, 2.8, and 2.9 yield as the approximate h-parameters of the compound:

$h_{fe} \approx 1300$ $h_{ib} \approx 52$ Ohms

The high frequency effective load impedance of the first stage is 5.16 kOhms. Similarly, the effective low frequency load impedance is 11.7 kOhms. From these load impedance values the gains may be calculated. Equation 2.5 gives an approximate high frequency gain of 40 and a D.C. gain of 90.

The low frequency input impedance can be calculated from equations 2.6. The resulting value is 168 kOhms. Series base resistors R_4 and R_5 increase the actual input impedance at D.C. to about 200 kOhms but they also decrease the D.C. gain by about 15%.

Resistors R_4 and R_5 are required for three reasons. They help to reduce the temperature dependent drift of the input stage; they isolate the summing junction from the input capacity of the input stage; and they raise the effective closed loop source resistance for the input stage. Their values should not be more than 33 kOhms since the corner frequency they produce with the input capacity must occur well beyond the unity gain frequency of the input stage.

If no biasing arrangement is included to supply the quiescent base current for Q_4 this current will be supplied by the output through the feedback network used with the amplifier. If the amplifier is used as a summer this will cause a non-zero output for zero input voltage to the amplifier. If the amplifier is used as an integrator, the required base current will come from the integrator capacitor and will discharge it at an excessive rate. The quiescent base current for Q_4 (figure 13) is therefore derived from an adjustable voltage divider through a very large resistor R_{10} which acts as a current source.

OVERALL AMPLIFIER RESPONSE

From the response of each stage the expected frequency response curve of the entire amplifier may be derived.

The D.C. gain of the amplifier is the product of the stage gains derated by 15% on account of the series base resistors in the input stage. The D.C. gain thus calculated is 74,000. The frequency response depends mainly on the roll-off networks and the feedforward gains of each stage. However, since the gain of the regular inputs of the second and third stages are not constant but depend on the impedance of the feedforward networks, small deviations occur. If the data calculated in the previous sections are supplemented by calculations based on formulae 2.15 to 2.21, the complete asymptotic frequency response curve can be derived. The results are depicted in figure 14. In this figure, two sloping sections occur which do not exhibit the conventional slopes of 20 or 40 dB per decade. This results from the fact that a decrease in regular input gain accounted for by a feed-forward network impedance increase is accompanied by an increase in input impedance to the regular input. Such an impedance increase causes a partly compensating gain change in the previous stage. The theoretical results of figure 14

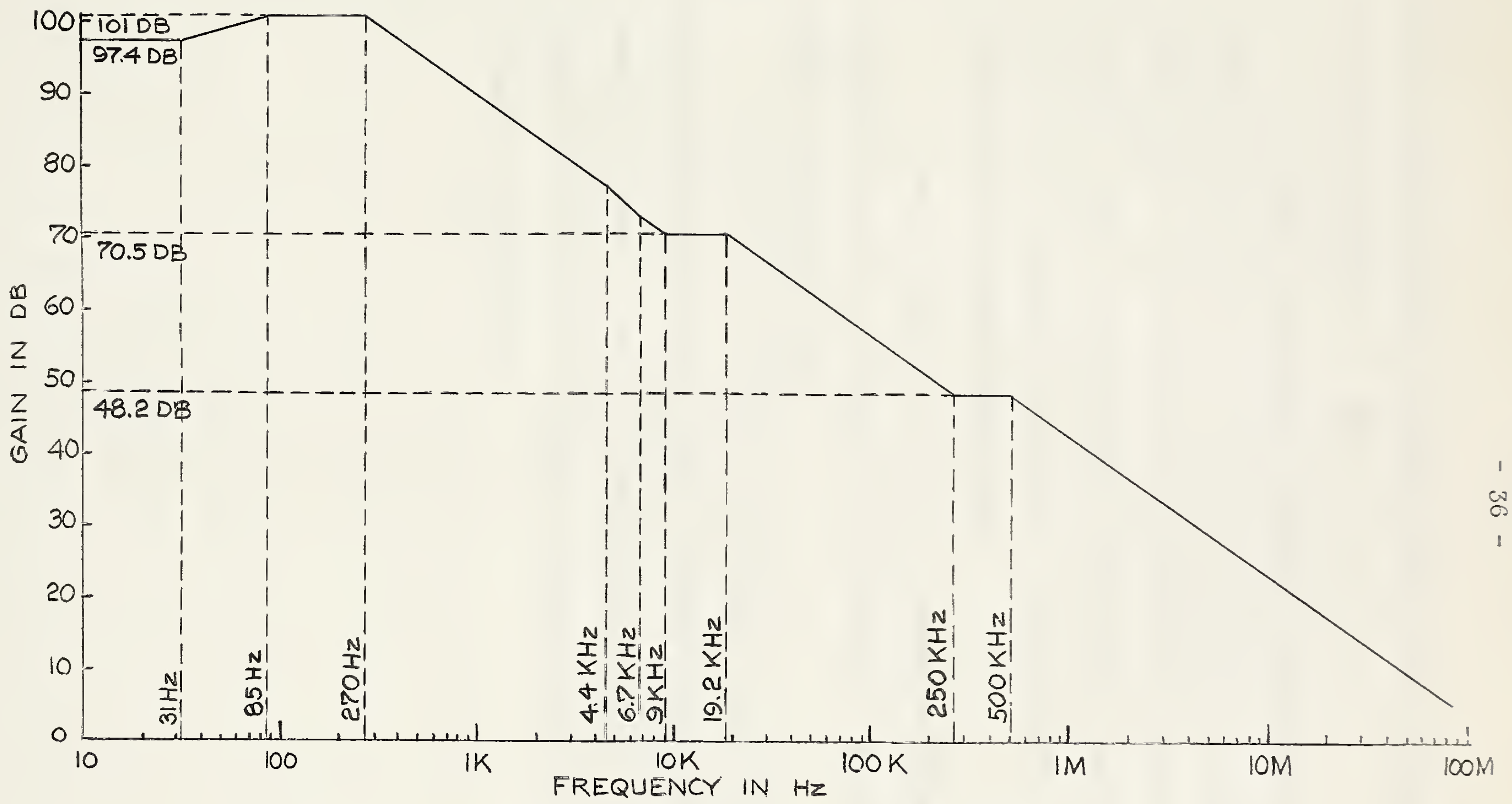

FIGURE 14. EXPECTED AMPLIFIER FREQUENCY RESPONSE

may be checked against the actual test results presented in a later chapter.

To obtain the response predicted theoretically, the amplifier was constructed on an epoxy laminated printed circuit card. The circuit was miniaturized as much as possible to keep all lead lengths short since long leads would introduce parasitic impedances that impair the operation at very high frequencies.

To keep integrator drift to a minimum, feedforward capacitors C_2 and C_4 (figure 13) were chosen to be mylar rather than ceramic units.

No transistor selection was carried out for the second, third, and output stages. However, the input transistors were selected for matching beta values and somewhat matching base to emitter voltage values at the collector currents used.

CHAPTER THREE

THE CHOPPER STABILIZER CHANNEL

The temperature dependent drift of the operational amplifier previously described may be too high for some applications. This temperature sensitivity can be greatly reduced by adding an additional amplifier channel in a feedforward scheme (figure 15).

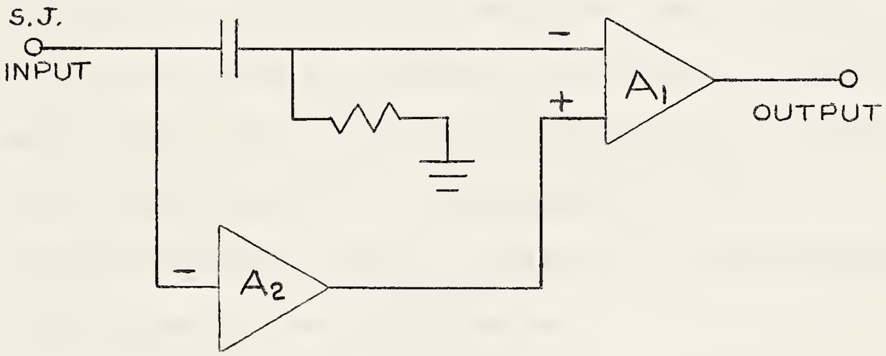

FIGURE 15. FEEDFORWARD SCHEME FOR TEMPERATURE SENSITIVITY REDUCTION

Amplifier A_1 is the main operational amplifier with differential input stage described previously. Use of the scheme in figure 15 leaves the high frequency gain unaltered and equal to $-A_1$. The D.C. and low frequency gain becomes approximately $-A_1A_2$ in agreement with feedforward theory. If amplifier block A_2 has no inherent

drift, then the drift of the entire amplifier is equal to the drift of A_1 divided by the gain of A_2, where all drift figures are referred to the inputs. Amplifier A_2, separately, therefore needs to be designed to have a very low drift figure.

To achieve a very low drift design for amplifier section A_2 the usual method is to amplitude modulate the D.C. input signal onto a carrier by means of chopping of the input signal. The resulting periodic signal is subsequently amplified in a driftless A.C. amplifier, demodulated again, and finally filtered to retrieve the original but amplified input signal. The modulator and demodulator are normally of the synchronous type so that polarity as well as amplitude information may be transmitted. The arrangement block diagram is shown in figure 16.

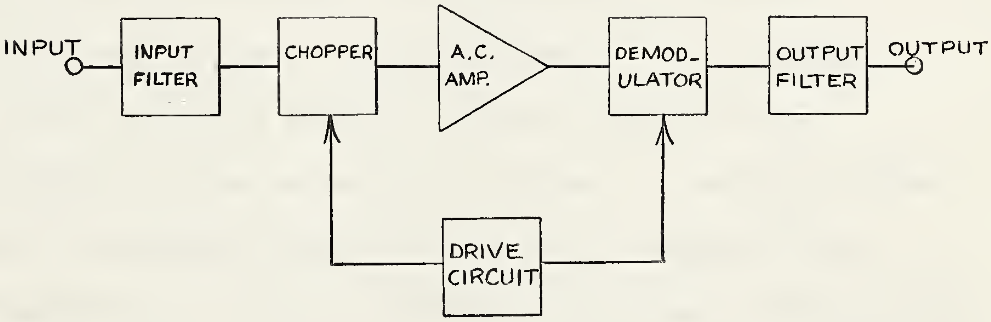

FIGURE 16. CHOPPER AMPLIFIER BLOCK DIAGRAM

A circuit of this type can still produce temperature dependent drift. Some of the causes would be:

1. The modulator produces an offset voltage, i.e. an output signal for zero D.C. input signal. The offset voltage may be the result of feedthrough of the drive signal into the main signal path, spurious electromotive forces, and switching spikes. Usually offset voltages produced in these ways are temperature sensitive.
2. A constant modulator offset voltage is amplified by the A.C. amplifier. If the gain of the A.C. amplifier varies with temperature, then the amplified offset produces a variable demodulated output which depends upon temperature.

The low drift properties of a chopper amplifier thus depend primarily on the characteristics of the chopper and upon the gain constancy with temperature of the A.C. amplifier. The most important features of the chopper should be that it produce no offset voltage and that switching spikes be kept to a minimum. If switching spikes are unavoidable, they should not vary in amplitude with temperature. There are several other chopper characteristics which may be temperature dependent, such as turned-on resistance, turned-off resistance, and mark to space ratio. However,

the latter characteristics will only affect the chopper efficiency and thus the chopper channel gain. These effects are usually of no consequence in a feedback system.

There are a number of devices, mechanical, optical, or solid state, which are useful as choppers, but each of these exhibits shortcomings peculiar to the individual device. For the purposes of this project, a solid state device was chosen because it offers long life and reliability, immunity from mechanical disturbances, and the possibility of operation over a wide range of driving frequencies.

In particular, a field effect transistor device was chosen because in a switching mode of operation it is a purely resistive device. However, the finite gate to channel resistance, though high, still injects a small portion of the driving signal into the main signal path thus producing an offset voltage. Also, the gate to channel capacity differentiates the driving signal and produces switching spikes. These switching spikes are of unpredictable amplitude because the gate to channel capacity depends upon temperature and gate to source voltage.

To alleviate these difficulties somewhat, the finally selected device for chopper operation is an insulated gate field effect transistor or MosFet. The MosFet has a gate to channel leakage resistance that is approximately two

orders of magnitude higher than for the regular field effect transistor. Furthermore, its gate to channel capacity is small and was found, by measurement, to be practically independent of temperature and operating voltages. The MosFet, therefore, is well suited to chopper operation.

As can be seen from figure 16, the chopper amplifier consists of an input filter, a modulator or chopper, an A.C. amplifier, a demodulator, and an output filter. A drive circuit for the chopper and demodulator is also included. The complete chopper amplifier circuit diagram is shown in figure 17.

Figure 15 shows that the chopper amplifier gain is required to be negative. The polarity of the gain depends on the phasing of the modulator and demodulator drive and on the polarity of the gain of the A.C. amplifier. Figure 18 illustrates the modulation, amplification, demodulation scheme.

Since the chopper amplifier is intended to be used with a main operational amplifier in a feedforward arrangement, the frequency response characteristics of the chopper amplifier must be designed in accordance with feedforward theory. In particular, the amplifier frequency response should be such that the gain rolls off at 20 dB per decade close to the unity gain frequency. The unity gain frequency

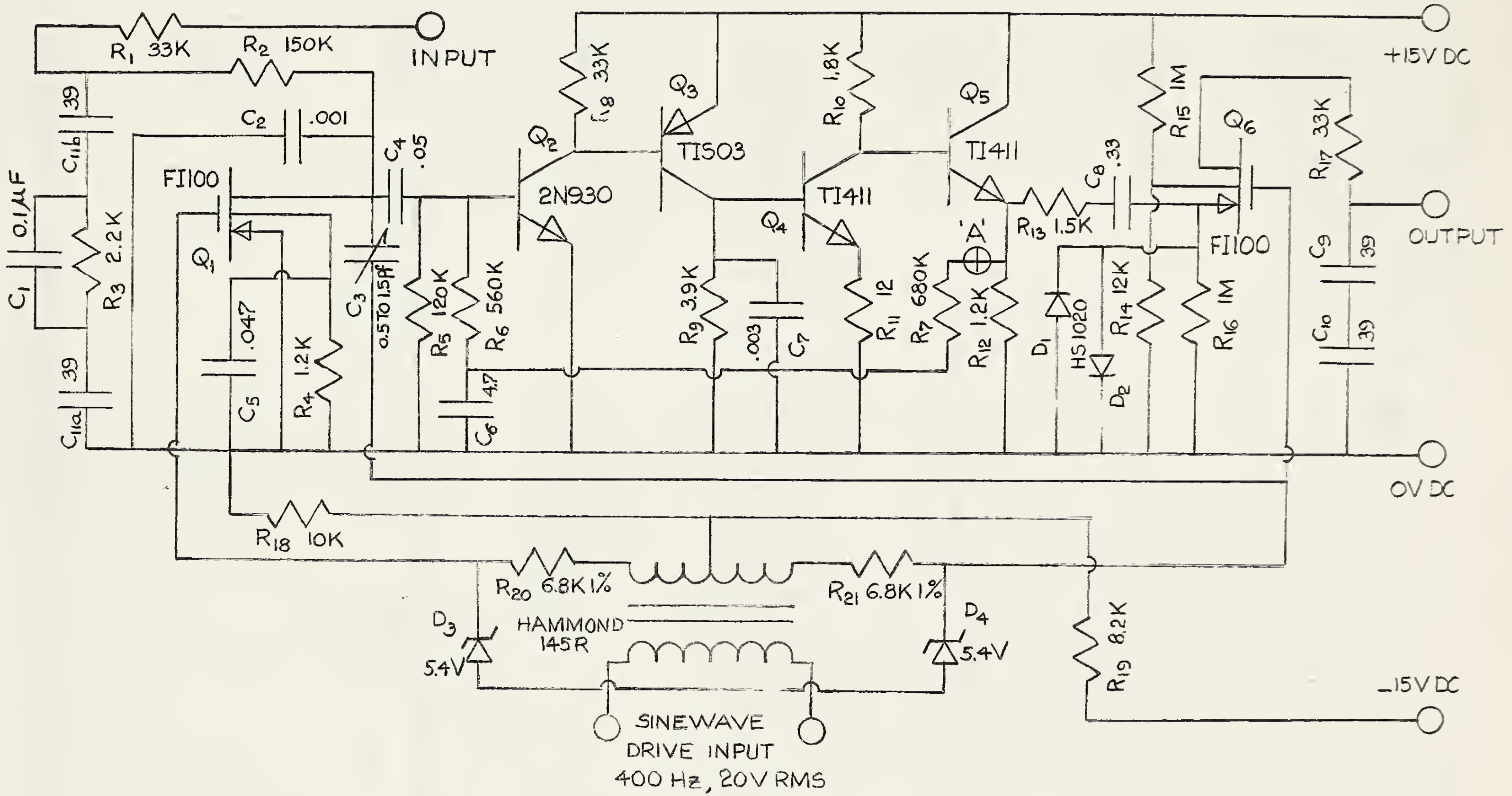

FIGURE 17. COMPLETE CHOPPER CHANNEL CIRCUIT

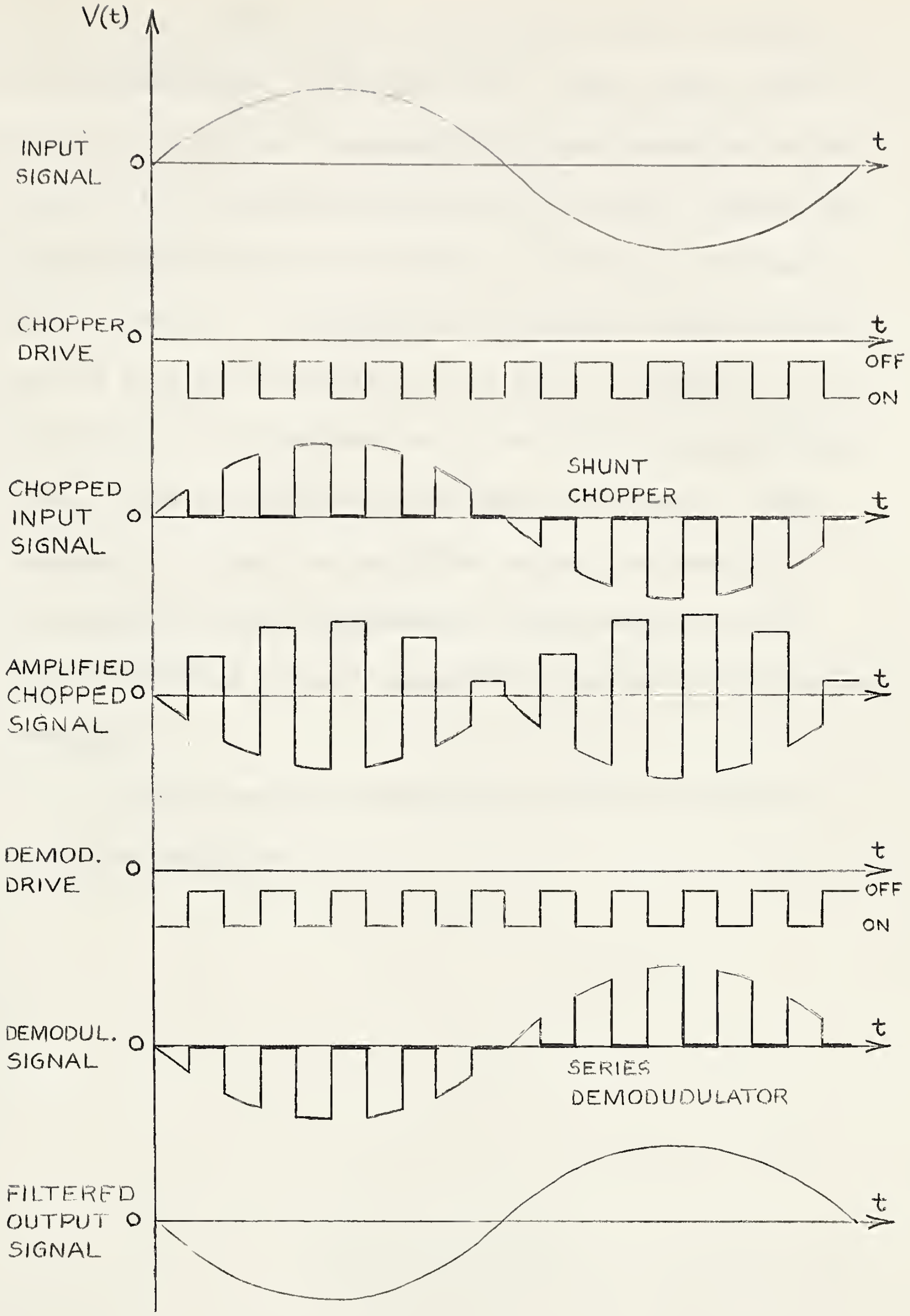

FIGURE 18. CHOPPER AMPLIFIER MODULATION-DEMODULATION SCHEME

should be one-fifth of the first major corner frequency of the main amplifier, which is 270 Hz. The output filter is made to roll off at a constant 20 dB per decade while the input filter response decreases at an initial slope of 20 dB per decade but which reverts to 0 dB before the unity gain frequency. The asymptotic frequency response curves for the filters and amplifier are shown in figure 19. In this figure, pole frequencies f_1 and f_3 for the input and output filters respectively are made to coincide. Zero frequency f_2 brings the amplifier slope back to 20 dB. The additional break frequencies f_n are caused by the input filter and the A.C. amplifier coupling and decoupling networks.

Further design considerations will be presented in subsequent sections.

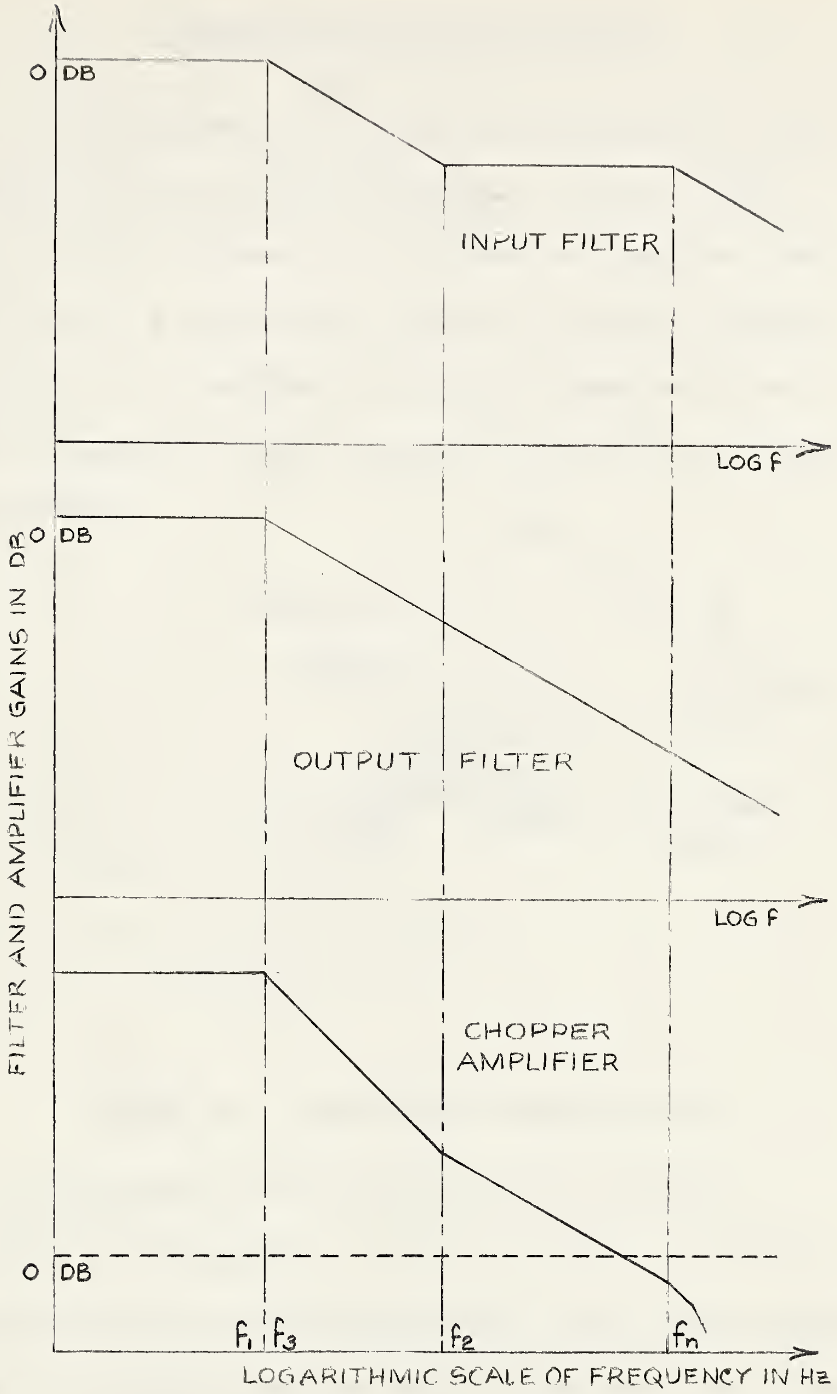

FIGURE 19. FILTER AND AMPLIFIER FREQUENCY RESPONSES

THE MODULATOR AND INPUT FILTER

The device used as a switch in the modulator is an insulated gate field effect transistor. For very small drain to source voltages, both positive and negative, the device acts as a gate voltage controlled variable resistor. This action is illustrated by the drain characteristics as shown in figure 20. Such a feature makes the device useful as a modulator.

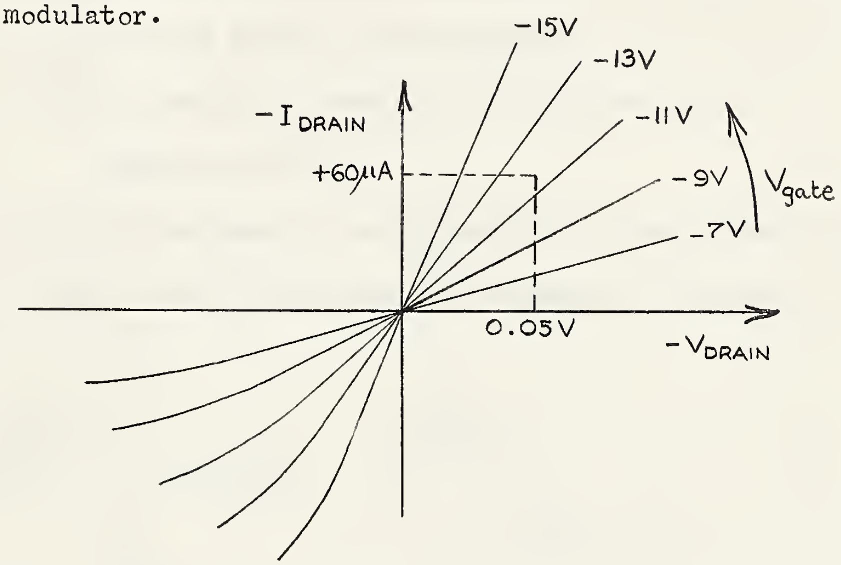

FIGURE 20. MOSFET DRAIN CHARACTERISTICS

Unfortunately, there are parasitic capacities associated with the MosFet. These capacities are the gate to source and gate to drain capacities, which cause switching spikes. Switching spikes are highly undesirable and efforts need to be made to minimize them as much as possible by suitable design.

The capacitors mentioned can be made less effective in producing switching spikes by using a shunt rather than a series chopper. In that case, only the gate to drain capacity is of consequence in the production of switching spikes.

The basic chopper configuration and its approximate equivalent circuit are shown in figure 21 where:

R_{on} is the MosFet on-resistance.

R_{off} is the MosFet off-resistance.

R_{in} is the input impedance of the first A.C. amplifier stage.

C_{gd} is the gate to drain capacity of the MosFet.

C_{str} is the wiring capacity in parallel with C_{gd}.

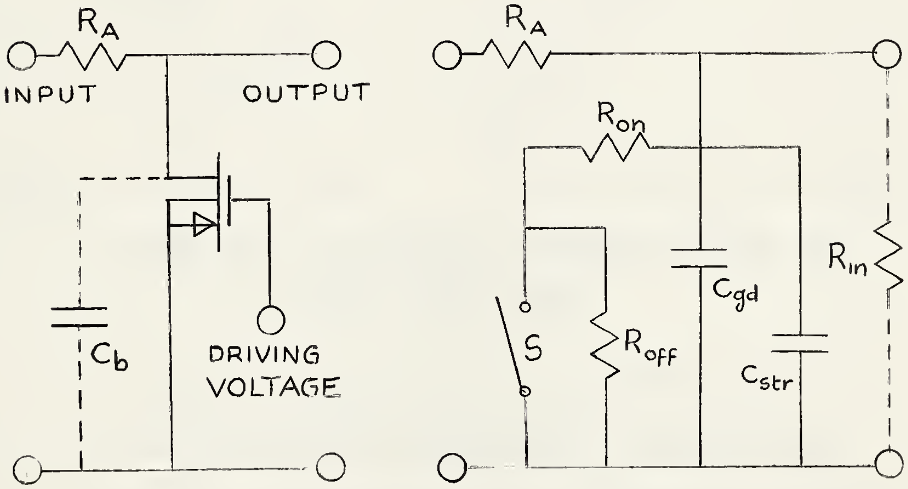

FIGURE 21. BASIC CHOPPER ARRANGEMENT AND ITS EQUIVALENT CIRCUIT

Generally R_{off} is very large and it can be assumed that $R_{off} \gg R_{in}$. If, also, R_{in} is selected such that $R_{in} \gg R_{on}$, then the approximate chopper efficiency η_1 is:

$$\eta_1 \approx \frac{R_A(R_{in} - R_{on})}{(R_{in} + R_A)(R_{on} + R_A)} \qquad \text{for: } R_{off} \gg R_{in}, \; R_{in} \gg R_{on} \tag{3.1}$$

For analysis of the switching spikes, the chopper circuit can be replaced by a suitable equivalent circuit and the driving voltage can be considered to be an imperfect step function. Figure 22 shows this.

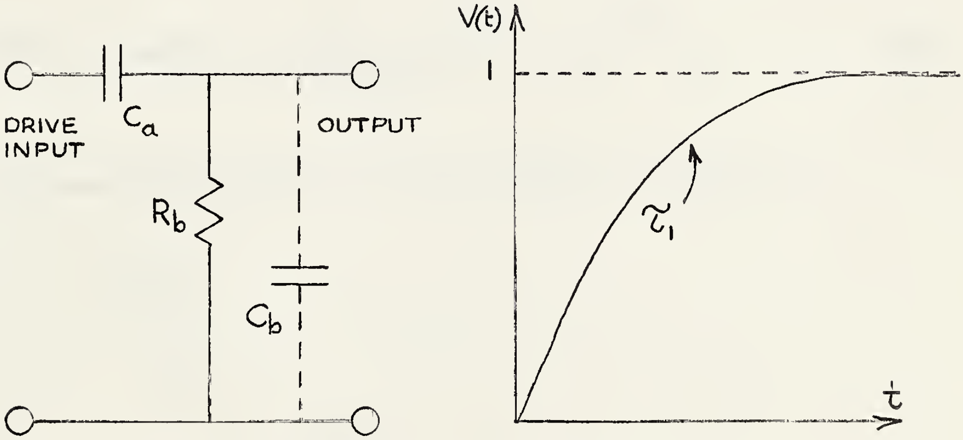

FIGURE 22. THE CHOPPER EQUIVALENT CIRCUIT AND DRIVE INPUT SIGNAL

For this equivalent circuit and drive input:

C_a is the parallel combination of C_{gd} and C_{str}.

R_b is the combination of all resistances from the output to ground.

The Laplace transform of the input voltage is:

$$V_{in}(s) = \frac{1/\tau_1}{s(s+1/\tau_1)} \qquad (3.2)$$

The transfer function of the circuit in figure 22 is:

$$G_1 = \frac{s}{s+1/\tau_2} \qquad \text{where: } \tau_2 = R_b C_a \qquad (3.3)$$

Therefore: $V_{out}(s) = G_1(s)\,V_{in}(s)$

$$= \frac{\frac{\tau_2}{\tau_2-\tau_1}}{(s+1/\tau_2)} - \frac{\frac{\tau_2}{\tau_2-\tau_1}}{(s+1/\tau_1)} \qquad (3.4)$$

Thus: $$V_{out}(t) = \frac{\tau_2}{\tau_2-\tau_1}\left\{e^{-t/\tau_2} - e^{-t/\tau_1}\right\} \qquad (3.5)$$

The resulting switching spike appears in figure 23.

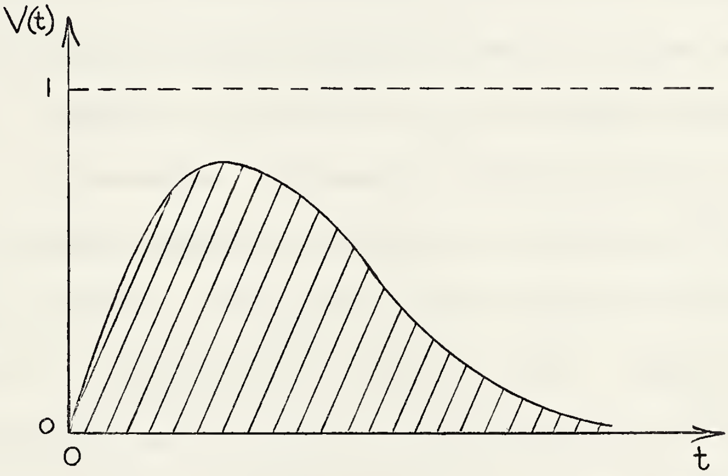

FIGURE 23. THE SWITCHING SPIKE

The amplitude of the switching spike may be reduced by putting a capacitor C_b in parallel with the chopper (figures 21, 22). The new transfer function is then:

$$G_2(s) = \frac{C_a}{C_a + C_b} \cdot \frac{S}{S + 1/\tau_3}$$

$$\text{where: } \tau_3 = R_b(C_a + C_b) \tag{3.6}$$

From the similarity between $G_1(s)$ and $G_2(s)$ it is easily concluded that the new spike voltage is:

$$V_{out}(t) = \frac{C_a}{C_a + C_b} \left\{\frac{\tau_3}{\tau_3 - \tau_1}\right\} \left\{e^{-t/\tau_3} - e^{-t/\tau_1}\right\} \tag{3.7}$$

or:

$$V_{out}(t) = \frac{C_a R_b}{R_b(C_a + C_b) - \tau_1} \left\{e^{-t/\tau_3} - e^{-t/\tau_1}\right\} \tag{3.8}$$

This result shows that the spike amplitude is determined, for a given C_a, by R_a, τ_1, and C_b. Resistance R_b affects both the spike amplitude and the chopper efficiency. Therefore, reduction of R_b to any great extent offers no advantages. The same is partly true for the value of τ_1 although some spike reduction is possible if τ_1 is properly selected. The greatest spike amplitude reduction, however, is effected by the addition of C_b. Capacitor C_b should be selected as large as possible without deteriorating the chopper output waveform too much. The best values of C_b, R_b, and τ_1 are most easily selected experimentally.

The offset voltage produced by the switching spikes is proportional to the area under the spike curve (figure 23). Subsequent filtering in the A.C. amplifier can reduce the spike amplitude further, but the area under the curve, and thus the offset voltage, is reduced very little by such measures.

A more powerful method of reducing the spike amplitude as well as the effective area under the curve is neutralization. Such neutralization is accomplished by feeding a signal, equal in magnitude and waveform to the chopper drive signal but of opposite phase, to the MosFet drain through a small trimmer capacitor. Both C_a and the neutralizing trimmer feed to the same varying impedance level. This produces two spikes equal in magnitude and waveform at all times but of opposite polarity. These spikes tend to cancel each other and the most effective neutralization occurs.

Neutralization is an additional reason for selecting a shunt rather than a series chopper. Had a series chopper been used, both C_{gd} and C_{gs} would have had to be neutralized separately. Neutralization of shunt choppers is simpler and more effective.

In the amplifier circuit shown, (figure 17) both neutralization and bypassing of the chopper by a capacitor

are used as methods of spike control. Capacitor C_3 is the neutralizing trimmer (approximately equal in size to C_a) and C_2 is the bypass capacitor.

The input filter performs two functions simultaneously. It must attenuate the high frequencies beyond the unity gain frequency and close to the carrier frequency and prevent them from entering the A.C. amplifier and demodulator; and it must isolate the summing junction or input from the carrier frequency components and switching spikes.

The analytically derived transfer function of the input filter (figure 17) is exceedingly complicated if the effects of C_2, C_4, and the A.C. amplifier input impedance are taken into consideration. The low pass filter effect can be approximated with more than sufficient accuracy by:

$$G_3(s) = \frac{R_3(C_1 + C_{11})s + 1}{R_1R_3C_1C_{11}s^2 + \{R_1C_{11} + R_3(C_1 + C_{11})\}s + 1} \qquad (3.9)$$

where:

$$C_{11} = \frac{C_{11a}C_{11b}}{C_{11a} + C_{11b}}$$

Substitution of numerical values and factorization allows the location of the poles and zeros to be determined. One of the poles should occur at a frequency higher than the unity gain frequency of the chopper amplifier.

In the reverse direction the input filter attenuates

the carrier frequencies since a pole occurs at a frequency equal to or lower than the major forward transfer function pole frequency depending upon the summing junction impedance.

Calculation gives the following results for the modulator and its input filter:

R_{in} = 50 kOhms (calculated later)

R_{on} = 1 kOhm (from MosFet data sheets)

Poles of $G_3(s)$ at: $f_1 = 0.25$ Hz; $f_4 = 700$ Hz.

Chopper and filter efficiency: $\eta_1 = 0.410$

D.C. input impedance: 180 kOhms minimum.

Zero of $G_3(s)$ at: $f_2 = 3.7$ Hz.

THE DEMODULATOR AND THE OUTPUT FILTER

The modulation-demodulation scheme depicted in figure 18 dictates the use of a series chopper if the modulator and demodulator are to be driven from out of phase waveforms. Such out of phase driving is desirable since in this manner the driving circuit outputs will be loaded equally, which helps to maintain equal waveforms for neutralization.

The MosFet used in the switching mode may be represented by a simple equivalent circuit as shown in figure 24. The drain characteristics for both positive and negative drain voltages with respect to the source are depicted in figure 25. The demodulator should respond

equally for both positive and negative output signals. However, as can be seen from figure 25, the characteristics are rather non-linear for drain voltages of plus 0.5 Volts with respect to the source. Such non-linearities impair the demodulator operation. Normally the two diodes in figure 24 are reverse biased and the gate to source voltage controls their turn-on characteristics. During reverse polarity operation of the MosFet, the diodes may become forward biased and the gate loses control of the turn-on characteristics.

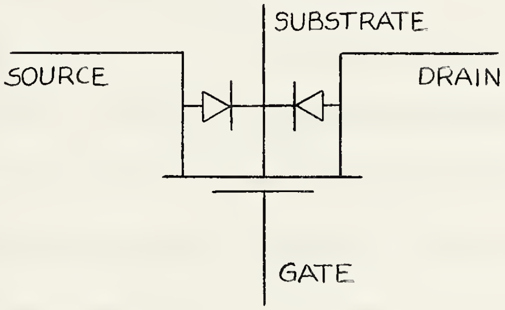

FIGURE 24. THE MOSFET SWITCH EQUIVALENT CIRCUIT

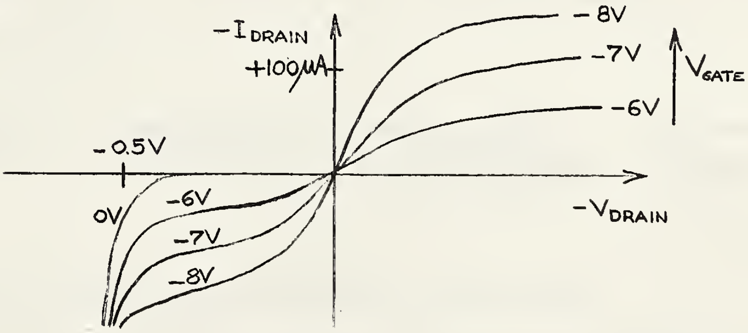

FIGURE 25. MOSFET DRAIN CHARACTERISTICS

The operation of the demodulator may be improved by returning the substrate connection to a positive voltage through a high impedance. This prevents the diodes from becoming forward biased and not being controllable by the gate voltage. Even if one of the diodes starts to turn on the high impedance limits the signal current that will flow to ground as a result. Resistors R_{15} and R_{14} in figure 17 represent the required substrate return connection. The demodulator is now reasonably linear for output voltages up to plus or minus 0.3 Volts.

Because the output signal levels are higher than the input levels by a factor of at least 1,000 neutralization of the demodulator switching spikes is unnecessary.

The output filter extracts the amplified input signal from the demodulator output and filters out the carrier frequency components. It also contributes to the amplifier frequency response roll-off characteristics.

Referring to figure 17, the transfer function of the output filter is:

$$G_4(s) = \frac{R_L}{R_{17} + R_{on} + R_L} \cdot \frac{1}{1 + \frac{(R_{17} + R_{on})}{R_{17} + R_{on} + R_L} \cdot \frac{C_9 C_{10}}{C_9 + C_{10}} \cdot s} \qquad (3.10)$$

where: R_{on} is the on-resistance of the MosFet

R_L is the load resistance across the amplifier output.

The D.C. attenuation or efficiency of the combined demodulator and output filter is:

$$\eta_2 = \frac{R_L}{R_{17} + R_{on} + R_L} \tag{3.11}$$

There are several additional efficiency factors associated with the amplifier operation.

The A.C. amplifier coupling networks eliminate the D.C. level of the chopper output signal (see figure 18). The efficiency factor of this process is $\eta_3 = 0.5$.

The demodulator extracts a modulated square wave with a D.C. offset voltage corresponding to the amplifier input signal from the A.C. amplifier output. The D.C. component of the demodulator output square wave is one-half of the peak value. The demodulation and filtering process, therefore, exhibits a basic efficiency of $\eta_4 = 0.5$.

Efficiency determinations have, so far, been based on a square wave modulator output. In actuality, the A.C. amplifier output is not a square wave because the chopper driving signal is not a perfect square wave and because the input filter and the A.C. amplifier distort the chopper waveform somewhat. The actual demodulator output waveform before filtering is shown in figure 26. Graphical analysis of the output waveform to determine the D.C. component and comparison with the D.C. component of an equivalent square

wave produces an additional efficiency factor $\eta_5 = 0.86$.

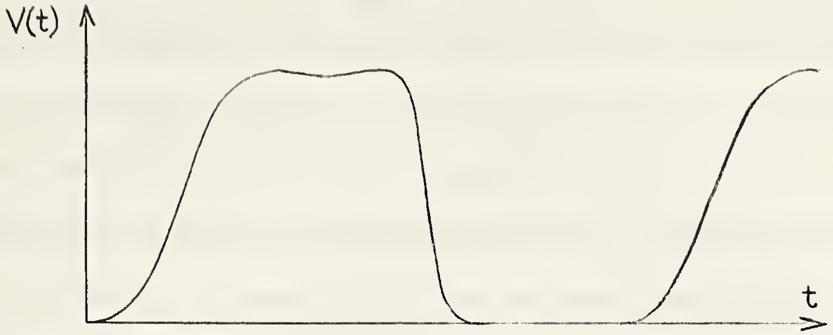

FIGURE 26. THE DEMODULATOR OUTPUT BEFORE FILTERING

The total efficiency η of the modulation, amplification, demodulation, filtering scheme is:

$$\eta = \eta_1 \times \eta_2 \times \eta_3 \times \eta_4 \times \eta_5 \qquad (3.12)$$

Substitution of numerical values into the formulae presented in this section produces the following results based on a MosFet on-resistance of 1 kOhm and an amplifier load resistance of 200 kOhms:

Demodulator and filter efficiency: $\eta_2 = 0.855$

Modulation-demodulation efficiency: $\eta = 0.0755$

Output filter pole at: $f_3 = 0.3$ Hz.

THE CHOPPER DRIVE CIRCUIT

To operate the modulator and demodulator MosFet switches, driving waveforms have to be applied to the MosFet gates. These waveforms are derived from the chopper drive

circuit.

The chopper requires two signals for its operation, one to be applied to the gate, the other for neutralization of the switching spikes. To make the neutralization effective, the driving and neutralizing signals must be of exactly equal waveform and magnitude but of opposite phase. The necessity for equality of the two waveforms, except for the phase difference of 180°, cannot be overemphasized. In addition to these requirements, the rise times of the leading and trailing edges of the waveform have to be controlled.

Many circuits of both the driven and self-excited variety were tried. The circuit shown in figure 17 produced the most nearly equal waveforms, especially at the edges which produce the spikes and which are therefore the most important.

In this circuit, two equal but oppositely phased sinewaves are derived from centertapped transformer T_1. These sinewave voltages are truncated by zener diodes D_3 and D_4, and resistors R_{20} and R_{21}. The centertapping of transformer T_1 was checked for balance. Equality of the signals was further maintained by use of carefully matched zener diodes and 1% tolerance resistors for R_{20} and R_{21}.

It is important not to over-drive the modulator since the spike amplitude is directly proportional to the drive amplitude. This is especially important during the chopper off period when the impedance levels are high. Both the drive amplitude and its D.C. level are therefore controlled. A gate voltage of minus 5 Volts will just turn the MosFets off, and minus 10 Volts will turn them on to an adequate on-resistance of 1 kOhm. The peak to peak drive voltage is equal to the zener voltage or 5.4 Volts. The drive circuit was therefore biased to minus 7.5 Volts by means of resistors R_{18} and R_{19} at the centertap of transformer T_1.

A special feature of the drive circuit is that each output is loaded by a MosFet gate. This helps to make the neutralizing output, which is the same as the demodulator drive output, more equal to the modulator drive voltage.

The rise and fall times of the chopper drive waveform may be set to an optimum value by varying the amplitude of the sinewave drive input. Use of a Hammond type 145R transformer allows driving directly off a 110 Volt, 400 Hz line with possibly a resistive voltage divider included for risetime control.

The allowable frequency range for the chopper

driving voltage is presently 250 Hz to 2 KHz. The optimum driving frequency is 400 Hz. Either higher or lower driving frequencies may be used but the A.C. amplifier coupling and decoupling networks as well as spike control capacitor C_2 will then have to be altered. The present frequency range was selected merely for convenience.

THE A.C. AMPLIFIER AND ITS COUPLING AND DECOUPLING NETWORKS

The A.C. amplifier must compensate for the low efficiency previously found for the modulation-demodulation process and it must provide the overall chopper amplifier gain of 1000. The required A.C. amplifier gain is thus $1000/\eta$ or about 13,000. A gain of this magnitude may easily be obtained from a simple three stage transistor amplifier with an emitter follower output stage.

The approximate gain of each common emitter stage is:

$$\text{V.G.} \approx \frac{R_L}{h_{ib} + R_E}$$

where R_L is the parallel combination of the collector resistor and the input impedance to the next stage, and R_E is the external emitter resistor, if any. The input impedance to each stage is approximately:

$$Z_{in} \approx \beta(h_{ib} + R_E)$$

The voltage gain of each stage is seen to depend markedly on h_{ib}. But, h_{ib} itself is a function of the collector current. The relationship is:

$$h_{ib} \approx \left(\frac{26 \text{ mV}}{I_c \text{ (in mA)}} + 1.5 \right) \text{ Ohms}$$

Referring to figure 17 the collector currents chosen for the stages are:

I_c for $Q_2 \approx$ 20 microAmps

I_c for $Q_3 \approx$ 0.2 mAmps

I_c for $Q_4 \approx$ 4.0 mAmps

Using these collector currents and assuming an average current gain β of 200 for transistors Q_3, Q_4, and Q_5, and a β of 100 for Q_2 (all measured average values) an A.C. amplifier gain of 13,600 is calculated. The calculated input impedance to the A.C. amplifier, R_{in}, is 130 kOhms.

The source resistance R_s for the input transistor (Q_2) varies between extremes of 1 kOhm and 180 kOhms. It is therefore difficult to arrive at an optimum collector current for Q_2 for low noise operation. A value of 20 microAmps was selected. Noise considerations dictate the use of a transistor type such as the 2N930 for the input stage.

As was pointed out earlier, it is necessary to keep the A.C. amplifier gain reasonably constant despite temperature variations. Since the gain depends on h_{ib} which in

turn depends on I_c it is important to keep the stage operating points as constant as possible. This is accomplished by using the D.C. output signal to control the bias level of the input stage and by direct coupling all stages. The biasing feedback path comprising resistors R_6 and R_7 (figure 17) needs to be restricted to low frequencies such that the normal A.C. gain of the amplifier will not be affected. Capacitor C_6 performs this function.

The RC input and output coupling networks help to eliminate the D.C. level from the chopper output. The corner frequencies for these networks must be chosen as low as possible in order not to deteriorate the chopper output waveform. However, their corner frequencies must be higher than the chopper amplifier unity gain frequency. The values of C_4 and C_8 were selected such that the break-frequencies are:

Input coupling network pole at: 35 Hz
Output coupling network pole at: 40 Hz

As a last consideration, it is required to limit the maximum signal amplitude to the demodulator in order not to overload it since this would produce undesirable side effects such as highly non-linear output signals, and long recovery time from amplifier overload. The limiting action is performed by two silicon diodes D_1 and D_2 across voltage divider

R_{13} - R_{16} (figure 17). The gain loss resulting from the use of the voltage divider was taken into consideration in the amplifier gain calculation. Some final adjustment in the amplifier gain may be made by changing resistor R_{11}.

CONSTRUCTION DETAILS

The entire chopper amplifier, including the drive circuit, was constructed on double sided copper and epoxy laminated circuit board. One side of the board was used for circuit wiring while the component side was used as a grounded shield.

To reduce the pick-up of extraneous drive signal frequency components, the amplifier sections were separated by vertical brass partitions soldered onto the circuit board. The connections between the drive circuit and the MosFet gates were etched out on the component side of the board in such a way that they were backed by grounded copper on the wiring side of the board. For further shielding, the entire circuit board was enclosed in a brass box. The terminals were brought out in strip form for insertion into edge connectors.

One test terminal corresponding to point 'A' in the circuit diagram (figure 17) was brought out so that, with the aid of an oscilloscope, the proper setting of neutralizing

trimmer C_3 could be checked.

Capacitors C_1, C_2 and C_4 were selected to be mylar capacitors since ceramic capacitors were found, by testing, to produce D.C. voltages when heated. Such voltages would produce temperature sensitive drift.

Test results on the chopper amplifier can be found in a later chapter.

CHAPTER FOUR

THE AMPLIFIER WITH A FIELD EFFECT TRANSISTOR INPUT STAGE

The operational amplifier described in chapter two has an input impedance of 200 kOhms and a D.C. gain of about 60,000. This means that for full output, a signal input current of 1 nanoAmp is required. Additionally, even though the quiescent bias current for the input stage is supplied from an internal current source, temperature variations may cause an unbalanced input current of 20 nanoAmps. Currents of this magnitude will quickly discharge a small integrating capacitor if the integrator is used in the holding mode.

The input current requirement may be considerably reduced by replacing the input transistor pair by field effect transistors. Use of field effect transistors in the input stage will not reduce the amplifier gain bandwidth product since the input stage, because of the use of feed-forward, amplifies only D.C. and low frequencies.

The second, third, and output stages of the amplifier described in this chapter are identical to those of the amplifier considered in chapter two. Design methods and calculations for the latter stages will not be repeated.

Although either field effect or insulated gate field effect transistors may be used for the purpose of

reducing the input current, this chapter will concentrate on the use of insulated gate field effect transistors or MosFets. However, only minor alterations are necessary if regular field effect transistors are to be substituted for the MosFets.

THE COMPOUND TRANSISTOR WITH MOSFET INPUT

Since the operational amplifier to be considered will use feedforward to later stages the input stage amplifies only D.C. and low frequency signals. Therefore, a simplified equivalent circuit, in which capacities associated with the MosFet are ignored, may be used. A convenient equivalent circuit is shown in figure 27, which uses conductance parameters to describe the properties of the device. On the basis of the internal operation of a MosFet it may be assumed without great loss in accuracy,(8) that $g_i = 0$ and $g_r = 0$.

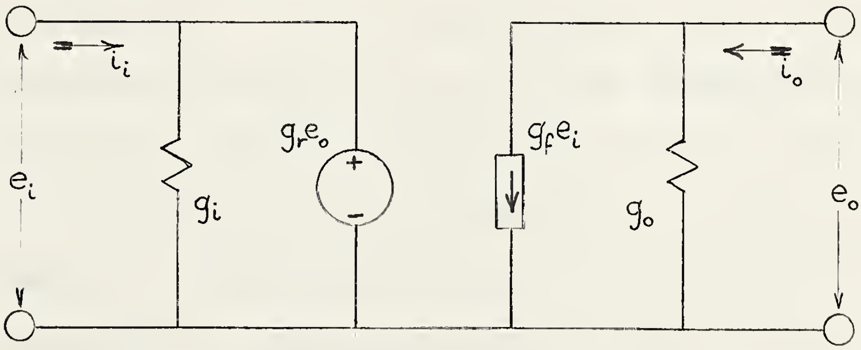

FIGURE 27. THE CONDUCTANCE EQUIVALENT CIRCUIT FOR A MOSFET

By employing the equivalent circuit shown together with the appropriate simplifying assumptions the following useful formulae (9) may be derived:

Output impedance of a source follower:

$$R_o = \frac{1}{g_f + g_o} \tag{4.1}$$

Voltage gain of a common source amplifier with an external source resistor R_{ss}:

$$V.G. = \frac{-g_f R_L}{1 + (g_f + g_o) R_{ss} + R_L g_o} \tag{4.2}$$

where R_L is the drain load resistor.

Output impedance of a common source amplifier with an external source resistor:

$$Z_o = \frac{(1 + g_f R_{ss})}{g_o} + R_{ss} \tag{4.3}$$

The input stage of this operational amplifier will be arranged in a manner similar to that used for the amplifier in chapter two. The first stage is, once again a differential arrangement, of which the gain and output impedance need to be calculated. The basic configuration is shown in figure 28.

To determine the single ended gain and the output impedance of transistor 2 in figure 28, the stage may be considered as a common source amplifier stage with an external source impedance equal to the output impedance of source follower transistor 1. The gain and output impedance

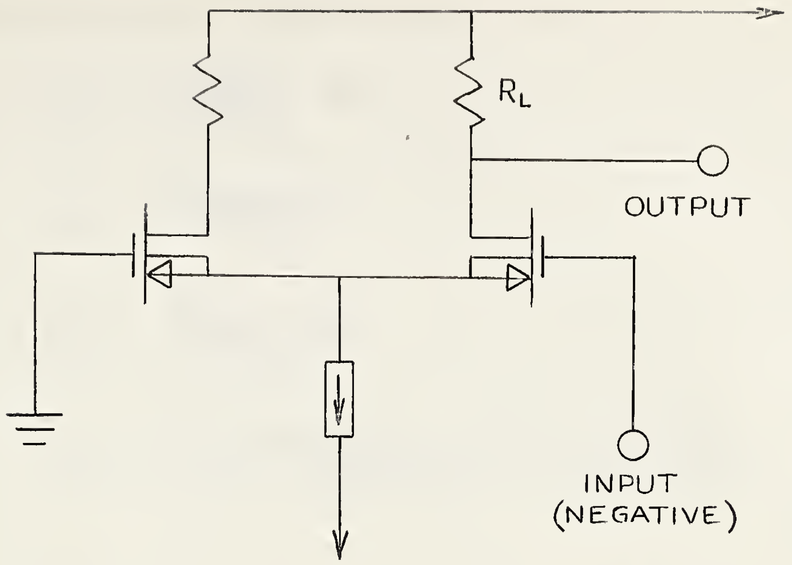

FIGURE 28. THE BASIC MOSFET DIFFERENTIAL STAGE

of the single ended differential stage are then obtained by replacing R_{ss} in equations 4.2 and 4.3 by R_o of equation 4.1. The results are:

Voltage gain: $$V.G. = \frac{-g_f R_L}{2 + R_L g_o} \tag{4.4}$$

Output impedance: $$Z_o = \frac{2}{g_o} \tag{4.5}$$

Actually, the differential stage will employ two compound transistors of the configuration shown in figure 29, which can be regarded as single MosFets with new equivalent conductance parameters.

Resistor R_A can be combined with transistor 2 in figure 29 to give a new set of h-parameters as follows,

obtained by using signal flow graph analysis:

$$h'_{ic} = \frac{R_A h_{ic}}{R_A + h_{ic}}$$

$$h'_{rc} = \frac{R_A h_{rc} + h_{ic}}{R_A + h_{ic}}$$

$$h'_{fe} = \frac{R_A h_{fc} - h_{ic}}{R_A + h_{ic}}$$

$$h'_{oc} = \frac{1 + h_{oc} R_A + h_{ic} h_{oc} - h_{rc} + h_{fc} - h_{rc} h_{fc}}{h_{ic} + R_A} \tag{4.6}$$

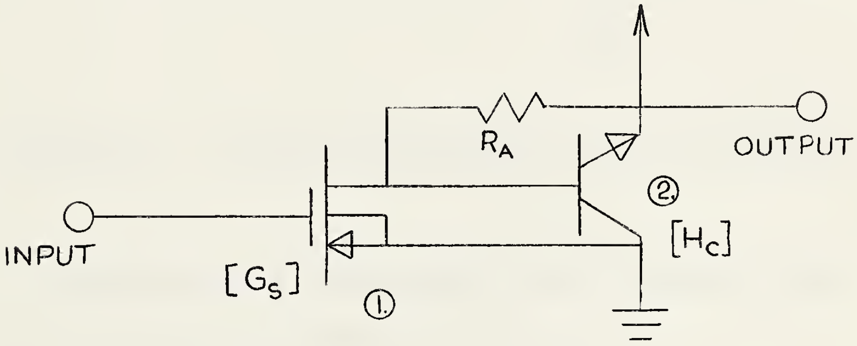

FIGURE 29. THE MOSFET COMPOUND TRANSISTOR

By using equations 4.6 the compound configuration can be simplified to that shown in figure 30. Equations can then be written for the circuit:

$$\begin{aligned} i_1 &= g_{is} e_1 + g_{rs} e_2 \\ i_2 &= g_{fs} e_1 + g_{os} e_2 \\ e_2 &= -h'_{ic} i_2 + h'_{rc} e_3 \\ i_3 &= -h'_{fc} i_2 + h'_{oc} e_3 \end{aligned} \tag{4.7}$$

where the G_s-parameters refer to transistor 1 and the H_c'-parameters refer to transistor 2 in figure 30. It was previously assumed that $g_{is} = g_{rs} = 0$. Therefore $i_1 = 0$.

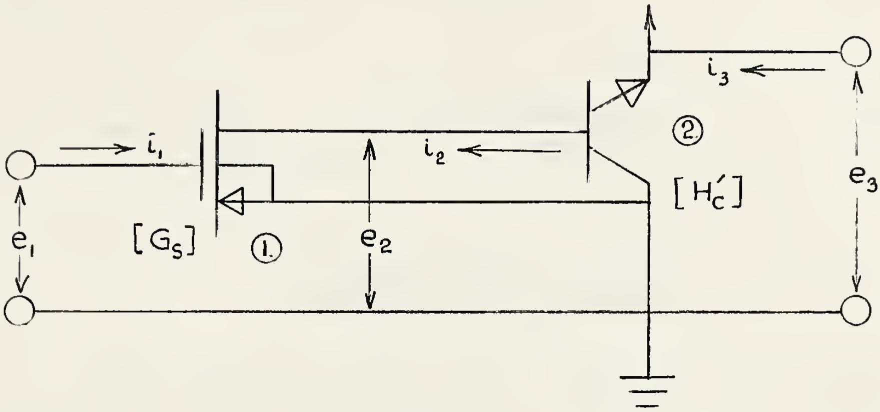

FIGURE 30. THE SIMPLIFIED MOSFET COMPOUND TRANSISTOR

The remaining equations may now be translated into a signal flow diagram as shown in figure 31.

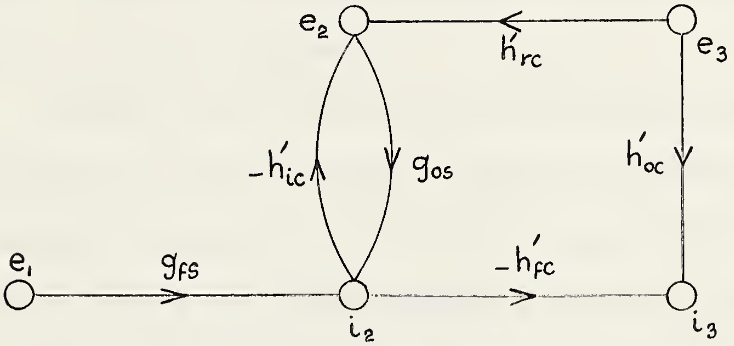

FIGURE 31. SIGNAL FLOW GRAPH FOR THE COMPOUND TRANSISTOR

Use of Mason's Rule on the flow graph of figure 31 yields the following results for the compound MosFet:

$$g_{fs}^{*} = \left.\frac{i_3}{e_1}\right|_{e_3 = 0} = \frac{-g_{fs}h'_{fc}}{1 + g_{os}h'_{ic}} \qquad (4.9)$$

$$g_{os}^{*} = \left.\frac{i_3}{e_3}\right|_{e_1 = 0} = h_{oc}^{1} - \frac{h'_{rc}g_{os}h'_{fc}}{1 + g_{os}h'_{ic}} \qquad (4.10)$$

THE OPERATIONAL AMPLIFIER

The circuit diagram of this operational amplifier is very similar to the arrangement used for the amplifier of chapter two. However, all pnp and npn transistors were exchanged for their opposite polarity duals in order to accommodate the MosFets which require a negative drain voltage. The amplifier operation is not affected by this measure. Figure 32 shows the complete MosFet operational amplifier circuit diagram.

Stages two and three and the output stage are essentially the same as those of chapter two except that the biasing resistors for the second stage are different since the MosFet input stage requires different operating conditions. To set the quiescent D.C. level of the input stage collector half-way between effective operating voltages, the biasing level of Q_6 (figure 32) was set to minus 3.8 Volts.

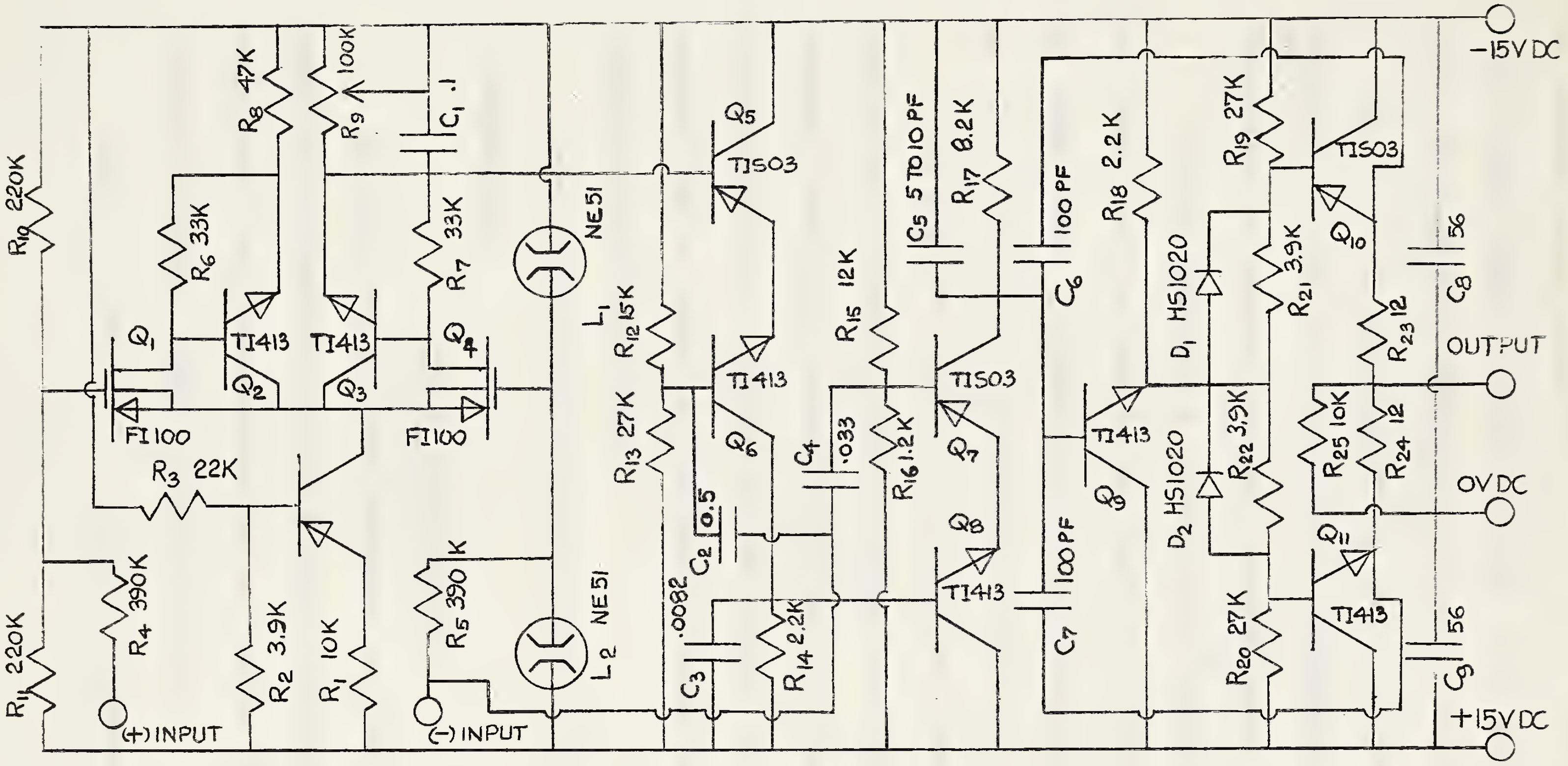

FIGURE 32. THE COMPLETE OPERATIONAL AMPLIFIER CIRCUIT WITH MOSFET INPUT STAGE

The current source resistors R_1, R_2, and R_3 were set to give a total input stage collector current of 190 microAmps per side. The MosFet drain current was set to about 20 microAmps per side, by means of resistors R_6 and R_7 (figure 32). These resistors may have to be adjusted to compensate for the differences in turn-on voltages from one MosFet to another.

Biasing resistors R_{10} and R_{11} are included to protect the MosFet gate insulation from puncture in those cases where the input is not grounded and electrostatic charges can build up. Neon bulbs L_1 and L_2 similarly protect Q_4.

The negative input of this amplifier does not require biasing from a current source to supply the quiescent input current. That input current is typically of the order of a few picoAmps and is allowed to flow through the feedback network from the output to the input, without causing operational amplifier error.

Other considerations are the same as for the amplifier of chapter two.

DESIGN CALCULATIONS

To carry out gain and impedance calculations, the equivalent g-parameters of the MosFet compound must be calculated. The g-parameters for transistors Q_1 and Q_4 at their operating points are (figure 32):

$g_{fs} = 200 \mu\text{mhos} \qquad g_{os} = 0.2 \mu\text{mhos}$

The h-parameters, at their operating points, for Q_2 and Q_3 are:

$h_{ie} = \beta h_{ib} = 10.7$ kOhms $\qquad h_{ic} = 10.7$ kOhms

$h_{re} = 1 \times 10^{-4}$ $\qquad h_{rc} = 1$

$h_{fe} = 70$ $\qquad h_{fc} = -71$

$h_{oe} = 3.5 \mu$mhos $\qquad h_{oc} = 3.5 \mu$mhos

The common collector h-parameters which include the effect of resistors R_A, as calculated from equations 4.6 are:

$h'_{ic} = 8.08$ kOhms $\qquad h'_{fc} = -54$

$h'_{rc} = 1$ $\qquad h'_{oc} = 3.5 \mu$mhos

Substitution of these parameters into formulae 4.8 and 4.9 produces the equivalent g^*-parameters for the compound as:

$g^*_{fs} = 10{,}800 \mu$mhos $\qquad g^*_{os} = 14.3 \mu$mhos

The output impedance of the input stage can now be calculated from equation 4.5 and is:

$Z_o = 140$ kOhms

Combining this with the drain load resistor gives a final output impedance of 35.2 kOhms.

The high frequency gain of either input of the second stage (Q_5 and Q_6 in figure 32) remains the same as that found in chapter two and is 13. The unity gain frequency of the input stage should, therefore, still be 9.6 KHz.

The bias network of the second stage is slightly different from that in chapter two. New values of D.C. gain and low and high frequency input impedance to the base of Q_5 result, as calculated from formulae 2.5 and 2.6. The D.C. gain is now 5.9, the low frequency input impedance is 15.5 kOhms and the high frequency input impedance is 5.8 kOhms. The effective low and high frequency load impedances that result are 11.7 and 5.16 kOhms respectively.

On the basis of the load impedance, formula 4.4 yields an imput stage D.C. gain of 58, while the high frequency gain becomes 29. The corner frequency of the input stage should thus be 9.6 KHz/29 or 330 Hz. The total parallel impedance level at the input stage drain is 4.98 kOhms at the higher frequencies. Roll-off capacitor C_1 can thus remain as 0.1 microfarads.

The new value for the frequency of the zero in the second stage feedforward gain, by formula 2.19, is 44 Hz, while the new low frequency feedforward input impedance is 7.8 kOhms. By the same reasoning as used in chapter two, feedforward capacitor C_2 is then required to be 0.5 microfarads. This concludes the MosFet amplifier design.

Except for the possibly slightly lower open loop D.C. gain, the frequency response characteristics of the MosFet input stage operational amplifier will be very similar to

those expected for the amplifier of chapter two. The same cautions and construction methods apply to this amplifier as to the previous one. Test results for this amplifier as well as those for the chopper stabilized amplifier of chapters two and three will be shown in chapter five.

CHAPTER FIVE

TEST RESULTS

After the amplifiers were constructed, performance tests were carried out on each amplifier. The basic tests that were performed, where applicable, are:

1. Measurement of D.C. open loop gain.
2. Frequency response of the amplifiers under conditions equivalent to open loop operation.
3. Square wave response, closed loop.
4. Determination of the maximum frequency at which full output voltage and current could be obtained (closed loop).
5. Integrator holding mode droop or voltage loss.
6. Closed loop frequency response and phase error.
7. Change in output voltage for zero input voltage (input shorted to ground) as a function of temperature.
8. Sensitivity of the output voltage to power supply changes.
9. Closed loop noise and distortion measurement.

The basic amplifier configuration for all of these tests is shown in figure 33. Open loop measurements were made on the closed loop amplifier by measuring the summing

junction voltage and comparing this to the output voltage.

The method of interconnection of the chopper amplifier and the planar input stage main operational amplifier for the purpose of chopper stabilization is shown in figure 34.

All test results are presented either in tabular or in graphical form.

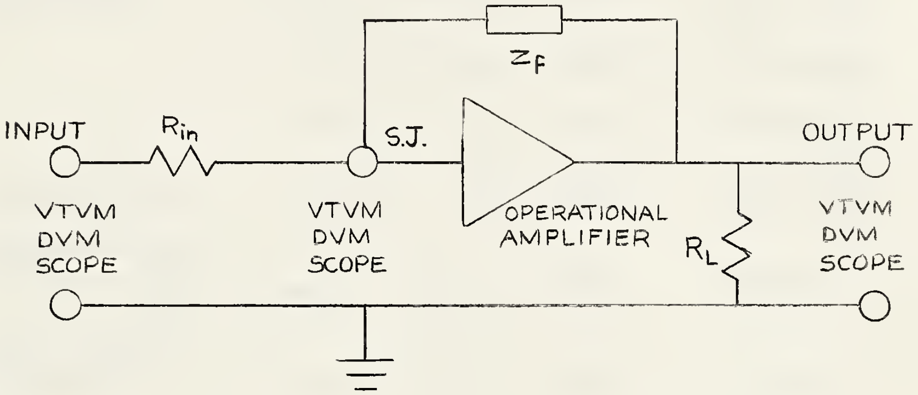

FIGURE 33. THE OPERATIONAL AMPLIFIER TEST ARRANGEMENT

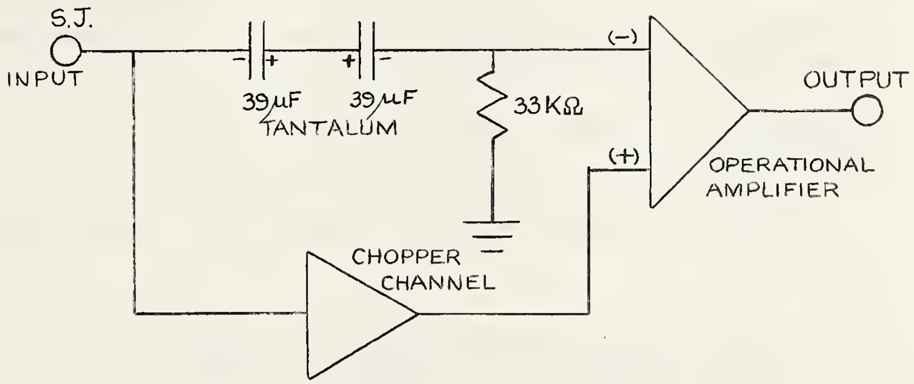

FIGURE 34. CHOPPER STABILIZATION CONNECTION

THE OPERATIONAL AMPLIFIER WITH PLANAR INPUT STAGE

MEASUREMENT	R_{in}	Z_f	R_L	RESULT
D.C. Open loop gain:	-	-	-	67,000
Square wave rise time:	100 kΩ	100 kΩ	470Ω	3.9 μsecs
	10 kΩ	10 kΩ	470Ω	0.34 μsecs
	1 kΩ	1 kΩ	470Ω	0.020 μsecs
Slewing rate:	1 kΩ	1 kΩ	470Ω	140 V/μsecs
Maximum freq. for full power	any	any	470	750 KHz
Max. freq. for 1/4 power:	any	any	470	1.5 MHz
Integrator discharge rate @ 10 Volts:	open	0.1μf	470Ω	20 mV/sec
Output change per supply change:	10 kΩ	10 kΩ	470Ω	-3 mV/V pos. supply
	10 kΩ	10 kΩ	470Ω	-1.5 mV/V neg. supply
RMS Noise:	10 kΩ	10 kΩ	470Ω	< 0.2 mV

TABLE 1. PLANAR AMPLIFIER TEST RESULTS

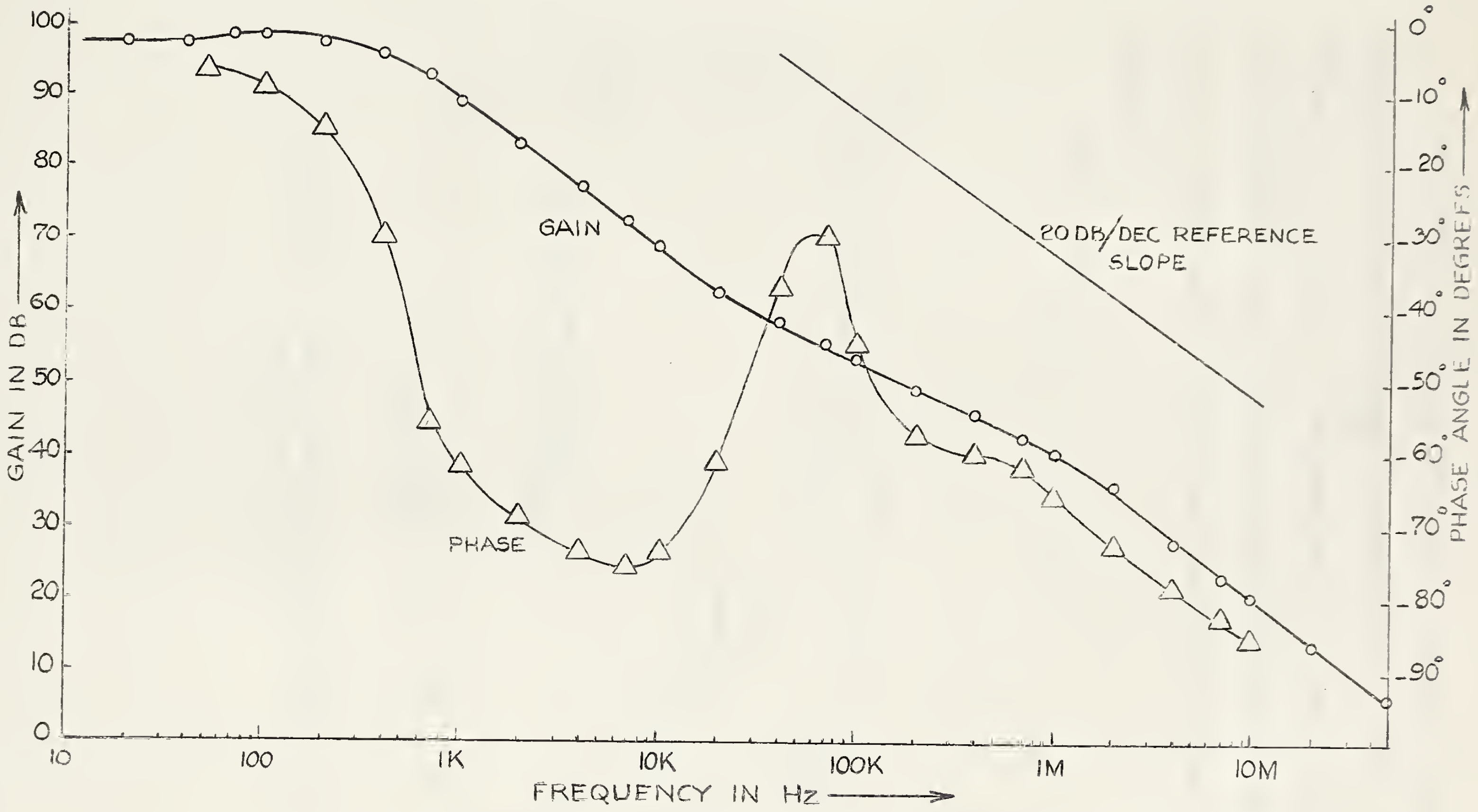

FIGURE 35. PLANAR INPUT AMPLIFIER FREQUENCY RESPONSE OPEN LOOP

The open loop and closed loop frequency responses are shown in figures 35 and 36 respectively. The output voltage as a function of temperature is shown in figure 37. The percentage total harmonic distortion versus frequency for full rated output voltage and current is shown in figure 38.

Table 1 shows all other results.

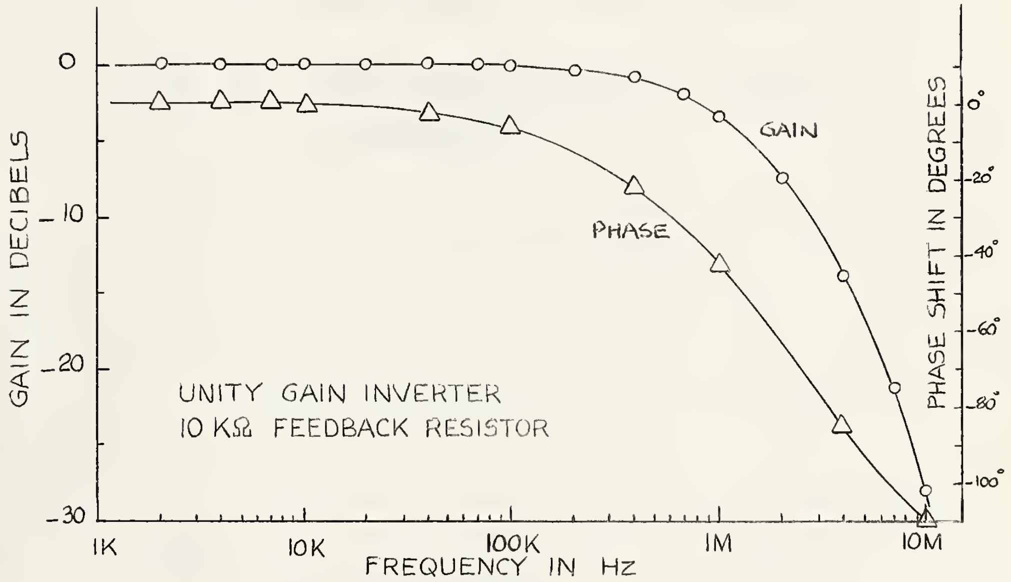

FIGURE 36. THE PLANAR AMPLIFIER CLOSED LOOP FREQUENCY RESPONSE

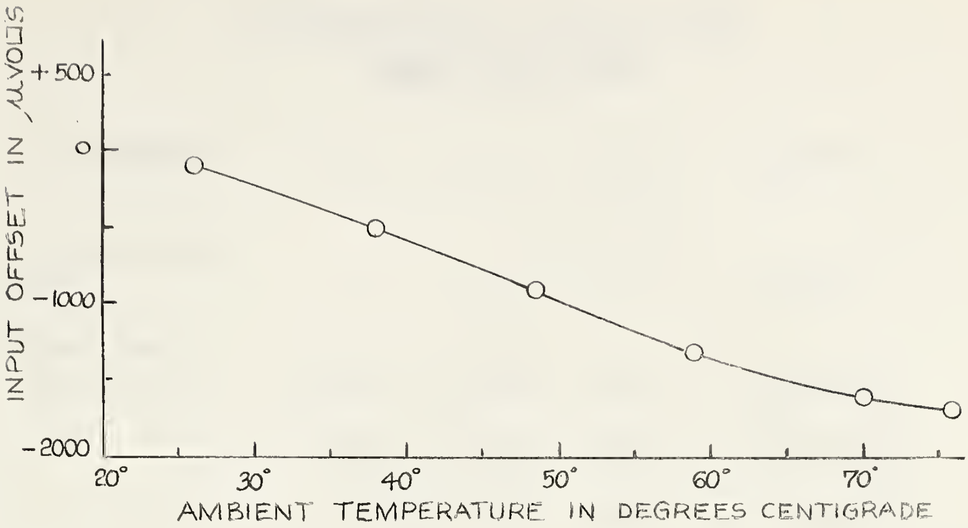

FIGURE 37. INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

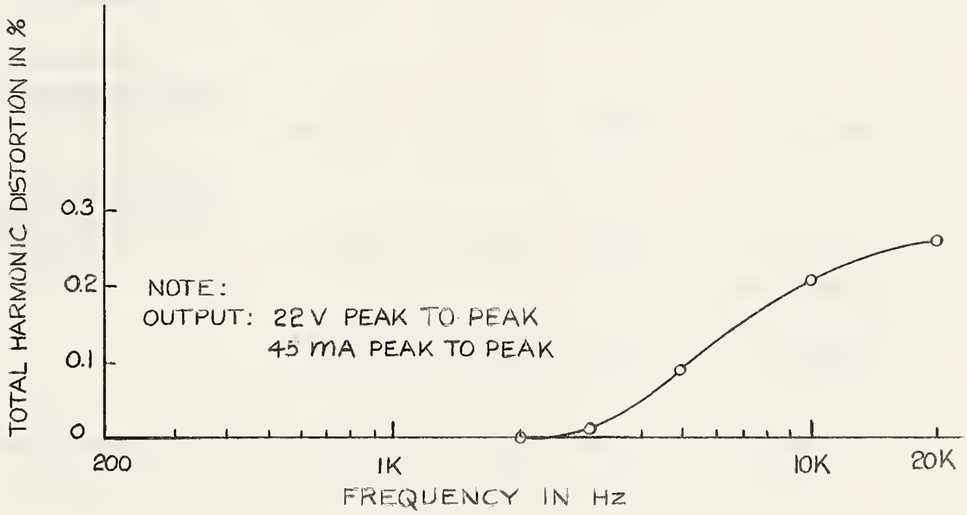

FIGURE 38. UNITY GAIN INVERTER TOTAL HARMONIC DISTORTION

THE OPERATIONAL AMPLIFIER WITH MOSFET INPUT STAGE

MEASUREMENT	R_{in}	Z_f	R_L	RESULT
D.C. Open loop gain:	-	-	-	62,500
Square wave rise time:	100 kΩ	100 kΩ	470Ω	2.8 µsecs
	10 kΩ	10 kΩ	470Ω	0.22 µsecs
	1 kΩ	1 kΩ	470Ω	0.014 µsecs
Slewing rate:	1 kΩ	1 kΩ	470Ω	200 V/µsecs
Maximum freq. for full power:	any	any	470Ω	750 KHz
Max. freq. for 1/4 power:	any	any	470Ω	1.5 MHz
Integrator discharge rate @ 10 Volts:	open	0.1µf	470Ω	1 mV/sec
Output change per supply change:	10 kΩ	10 kΩ	470Ω	1.5 mV/V pos. supply
	10 kΩ	10 kΩ	470Ω	0.2 mV/V neg. supply
RMS Noise:	10 kΩ	10 kΩ	470Ω	< 0.35 mV

TABLE 2. MOSFET AMPLIFIER TEST RESULTS

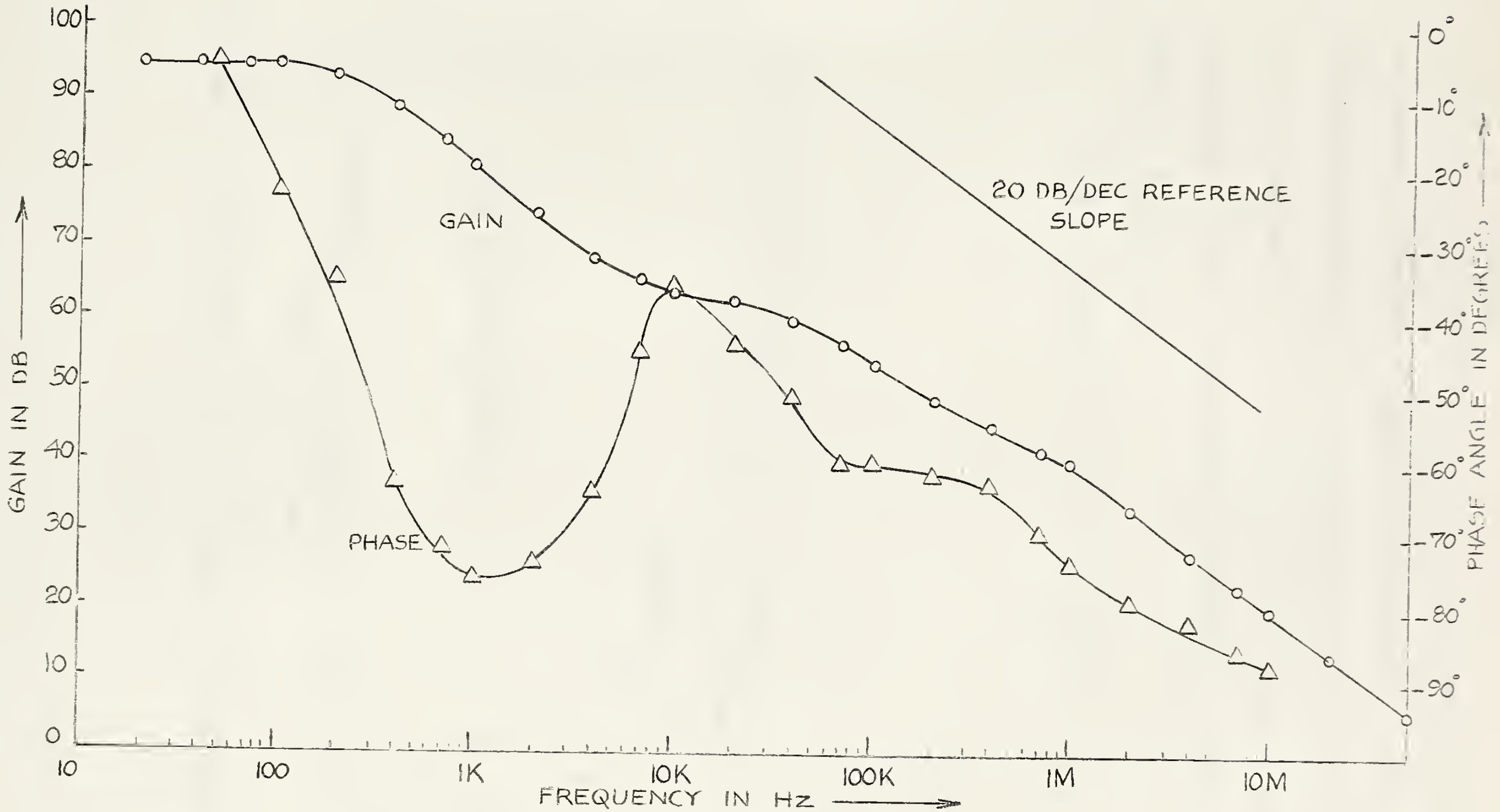

FIGURE 39. MOSFET INPUT AMPLIFIER FREQUENCY RESPONSE OPEN LOOP

The open loop and closed loop frequency responses are shown in figures 39 and 40 respectively. The output voltage as a function of temperature is shown in figure 41. The percentage total harmonic distortion versus frequency for full rated output voltage and current is shown in figure 42.

Table 2 shows all other test results.

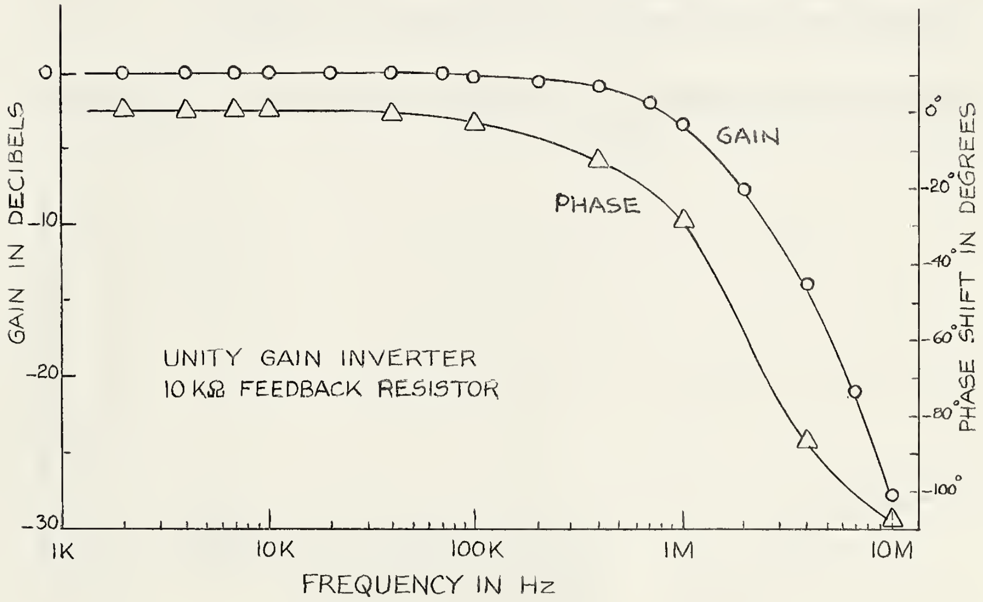

FIGURE 40. THE MOSFET AMPLIFIER CLOSED LOOP FREQUENCY RESPONSE

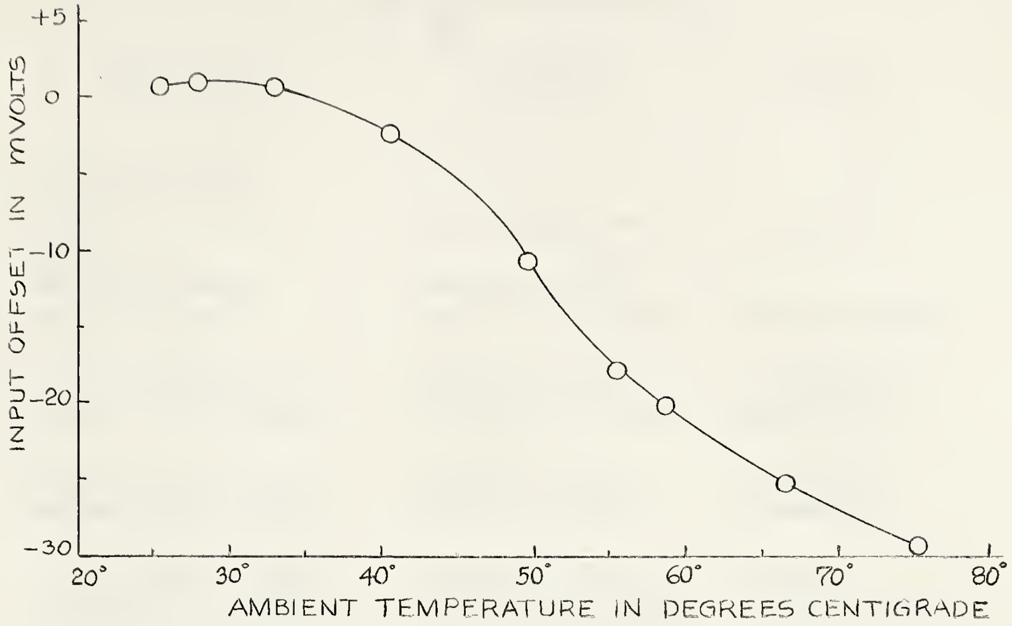

FIGURE 41. INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

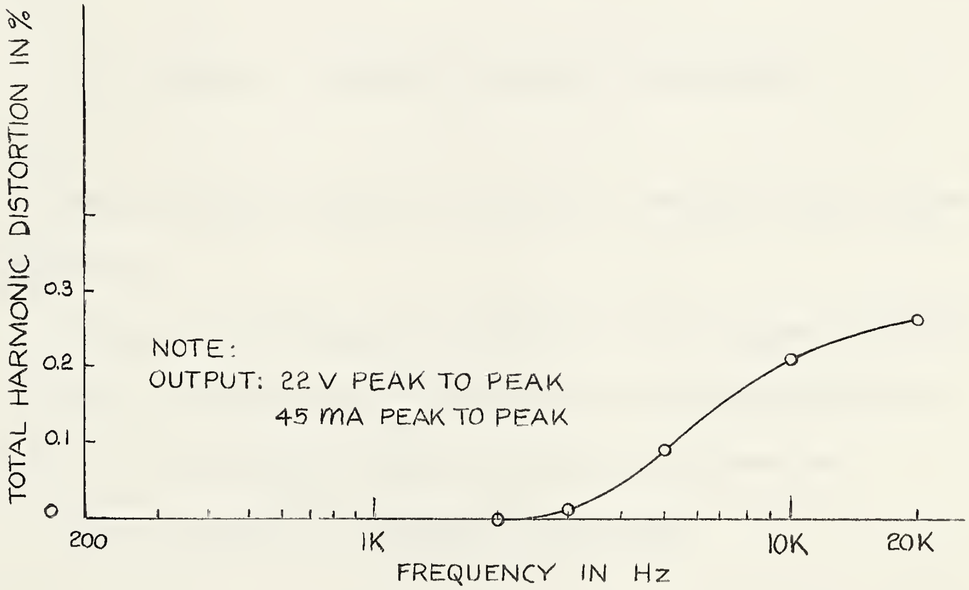

FIGURE 42. UNITY GAIN INVERTER TOTAL HARMONIC DISTORTION

THE CHOPPER AMPLIFIER

MEASUREMENT	CONDITIONS	RESULT
D.C. open loop gain:	R_L is 200 kOhms	1,000
Offset voltage w.r.t. input:	Chopper drive 400 Hz, 20 V RMS	Maximum 20 μV
Offset change for drive freq. change:	Chopper drive 200 Hz to 2 KHz	0.05 μV/Hz Maximum
Offset change for drive volt. change:	Chopper drive 20 to 25 V RMS	0.5 μV/V Maximum
Max. linear output voltage: R_L is 200 k	Chopper drive 400 Hz, 20 V RMS	plus or minus 0.25 V
Total peak to peak noise:	Chopper drive 400 Hz, 20 V RMS	Maximum 1 mV

TABLE 3. CHOPPER AMPLIFIER TEST RESULTS

The above test results all apply to the open loop chopper amplifier.

The open loop frequency response for the chopper amplifier is shown in figure 43, and the open loop temperature sensitivity of the offset voltage is plotted in figure 44.

Table 3 shows all additional test data.

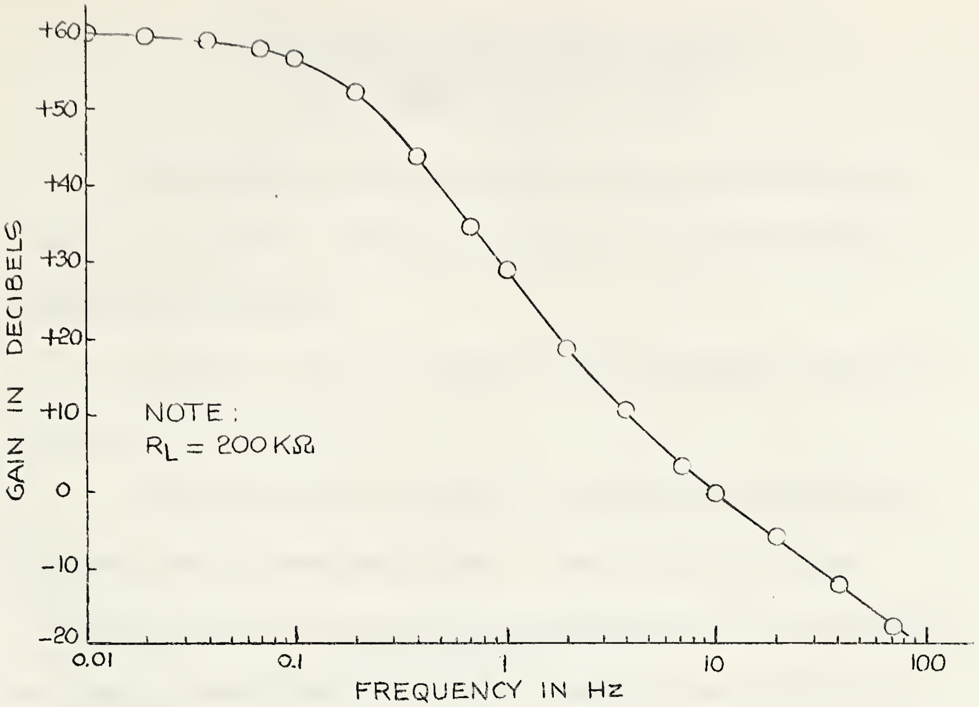

FIGURE 43. OPEN LOOP CHOPPER AMPLIFIER FREQUENCY RESPONSE

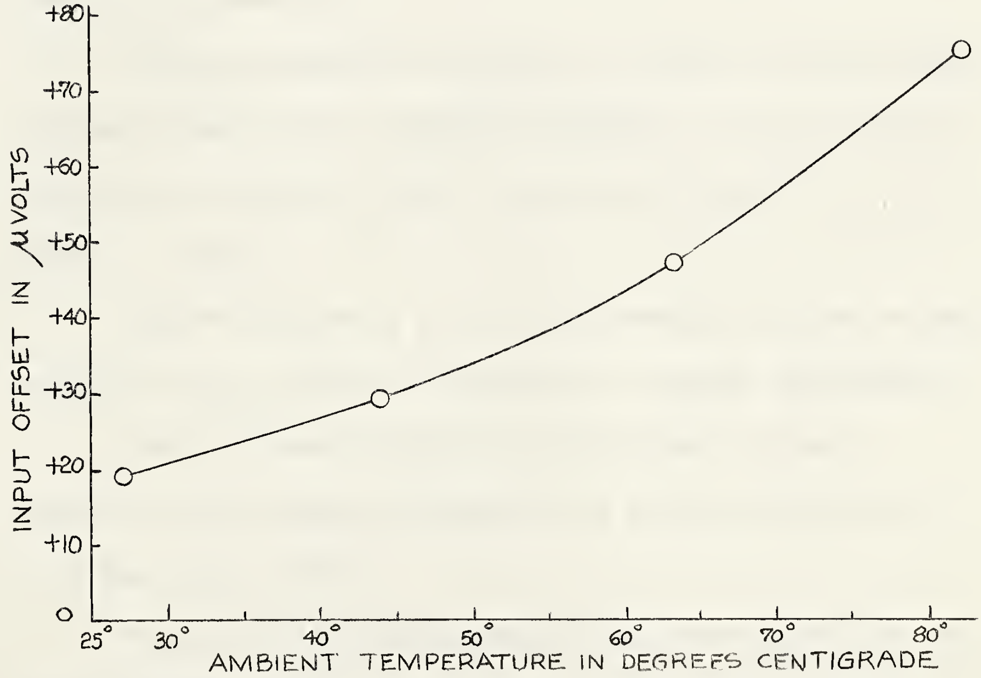

FIGURE 44. CHOPPER AMPLIFIER INPUT OFFSET VOLTAGE
AS A FUNCTION OF TEMPERATURE

THE PLANAR OPERATIONAL AMPLIFIER WITH CHOPPER STABILIZATION

The chopper stabilized operational amplifier was tested in a manner similar to that for the unstabilized operational amplifier.

The open loop D.C. gain of the stabilized amplifier was found to be 7×10^7.

The square wave response is essentially the same as for the unstabilized amplifier. From this it can be concluded that the high frequency response is not affected by chopper stabilization. As a result of the very high open loop gain the actual open loop frequency response could not be measured.

The sensitivity of the output voltage to power supply voltage changes for a unity gain inverter is plus 3 μVolts/Volt for the positive supply and plus 4 μVolts/Volt for the negative supply.

Figure 45 shows a plot of the change in offset voltage referred to the input as a function of ambient temperature.

The long term stability of the offset voltage referred to the input measured over a period of four hours is better than 1 μVolt.

The above temperature sensitivity data apply to a unity gain inverter.

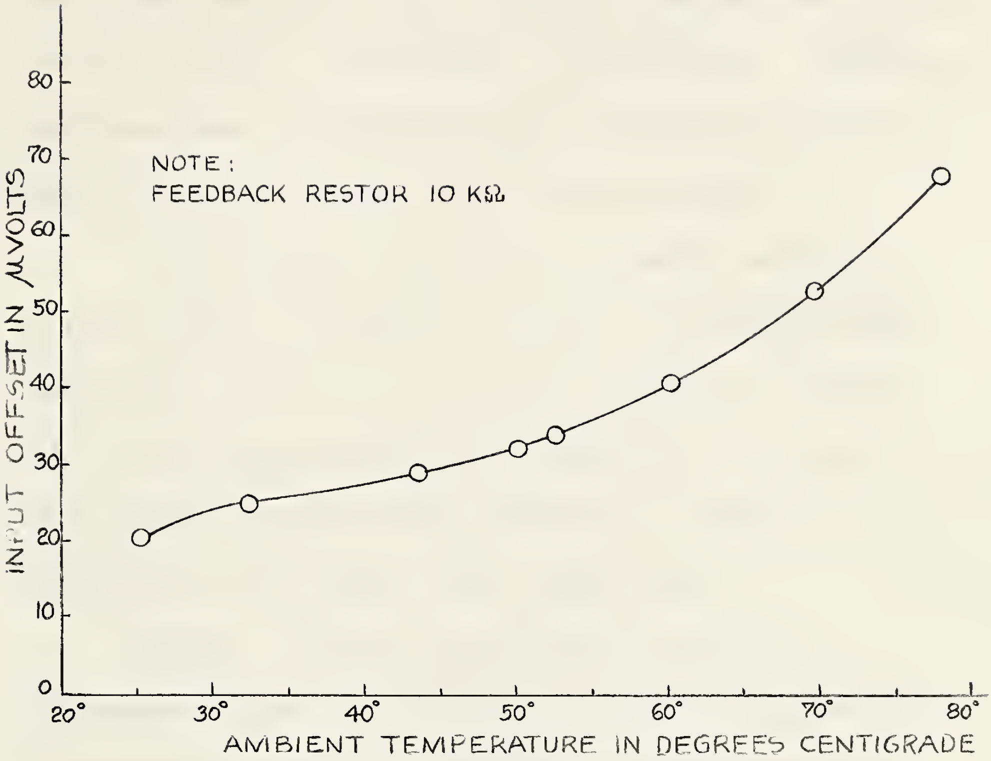

FIGURE 45. INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE FOR A CHOPPER STABILIZED UNITY GAIN INVERTER

CONCLUSION

This report has described the design of feedforward operational amplifiers with or without chopper stabilization and with a choice of two types of input stages. Feedforward techniques were used in the design of both the operational amplifier and the chopper stabilization channel.

The test results show that the design methods used do indeed make it possible to construct operational amplifiers with an open loop unity gain frequency of 100 MHz, while using readily available medium speed transistors. The frequency response characteristics are shown to be independent of the type of input stage used.

However, the test results also show that the frequency response of a unity gain inverter using one of the operational amplifiers described does not extend to frequencies as high as the open loop unity gain frequency. This is a direct result of the high amplifier input capacity associated with feedforward design. Nevertheless, good square wave response and rise times are still attained.

The amplifier input capacity may be reduced considerably if high frequency transistors with very small base to collector capacities are used in the third stages of the amplifiers. Until recently such silicon transistors with sufficiently high voltage ratings for use in these

amplifiers were not available.

As is evident from the test results, the selection of a field effect transistor input stage will improve the integrator holding mode operation by a factor of twenty. Very low frequency noise considerations, however, may prohibit the use of insulated gate field effect transistors in this application.

An alternative to the use of a MosFet input stage is chopper stabilization of the amplifier. The chopper design presented maintains the same amplifier D.C. input impedance while increasing the gain by one thousand times. The required low frequency input current is thus reduced and integrator holding mode operation is improved.

The use of chopper stabilization, using MosFets as modulator and demodulator switches, was shown to make it possible to construct an amplifier with an equivalent temperature sensitive input drift of less than one microVolt per degree Centigrade. Chopper stabilization using the design offered does not increase the output noise, as compared to the unstabilized amplifier.

The variety of designs presented in this report make it possible to select an all solid state operational amplifier best suited to a particular computational or general purpose problem.

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